RESEARCH PAPER

Predictive Physics Based Simulation of Nano Scale Gate-all-around Field Effect Transistor under the Influence of High-k Gate Dielectrics

Negin Moezi[1,], Mohammad Karbalaei[2]*

[1] *Department of Electronics, Technical and Vocational University, Kashan, Iran.*

[2] *Institute of nanoscience and nanotechnology, University of Kashan, Iran.*

ARTICLE INFO

ABSTRACT

In In this paper the electrical characteristics of a nano scale silicon gate-all-around field effect transistor (GAA-FET) with different dielectrics in the gate electrode are predicted. For this, we first calibrate physics based TCAD simulator against experimental results reported by IBM. Then the device electrical figures of merit comprised of I_{ON}/I_{OFF}, transconductance (g_m) and subthreshold slope (SS) are extracted. The obtained results show that utilizing various high-k gate dielectrics has a noticeable impact on the device performance. Different high-k gate dielectrics comprised of Al_2O_3, Si_3N_4 and HfO_2 are explored in our study. Moreover, when high-k gate dielectric is used instead of conventional SiO_2 insulator, the electrical characteristics will be improved in terms of I_{ON}/I_{OFF} ratio, transconductance to drive current ratio (g_m/I_{DS}) and SS. Based on our simulations and obtained results, scaling GAA-FETs by utilizing high-k dielectrics offers superior electronic devices and promising candidates for "more Moore" domain and integrated circuit applications.

How to cite this article

INTRODUCTION

To increase electrical performance in integrated circuit (IC), shrinking the size of transistors is aggressively performed. Although continuous scaling in semiconductor transistors can increase device density and performance, but appearance of short channel effects (SCE) and degradation of electrical characteristics of CMOS transistors in subthreshold region are unwanted results of scaling[1-7]. As gate oxide thickness reaches below one nanometer for enhancing device electrical performance aim, the problem of gate leakage current due to quantum tunneling along SiO_2 increases[2, 4].Therefore it is necessary to replace conventional SiO_2 insulator by a material with higher dielectric constant to increase gate oxide thickness while having excellent electrical performance. Recently, device designers have offered variety of materials, geometries and technologies to overcome aforementioned problems. Utilizing of 2-D materials [8-12], high-k dielectrics and device geometries comprising of tunnel FET (TFET)[13-21], FINFET and GAA-FET [22-28], are some of these suggestions.

In GAA-FET due to the fact that the gate electrode has surrounded the entire channel volume, gate electrostatic control over the channel region is higher compared to single gate, double gate, tri-gate and omega/pi-gate structures, electrical characteristics can be further improved[29, 30]. Thus, it is predicted that GAA-

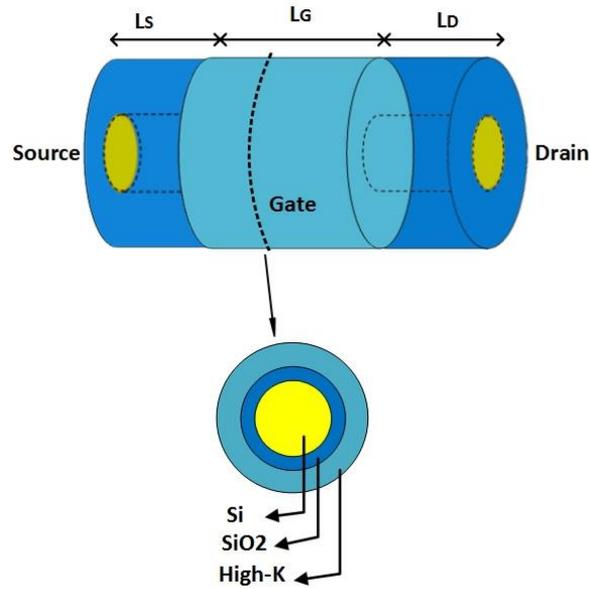** Corresponding Author Email: nmoezi@tvu.ac.ir*

Fig. 1. Schematic representation of GAA-FET under study with a circular cross section view.

FET can be a promising candidate with maximum capability to expand Moor's law[31]. However the main concern of GAA-FET is high OFF-current and subthreshold slope caused by scaling which limits the device performance for low power and steep switching applications[32]. Precise prediction and improvement in the electrical performance of ultra-short channel GAA-FETs necessitates taking quantum theory into account. This is due to the fact that quantum confinement and electron wave behavior is dominant in these devices[33].

In this work, we have considered a circular cross section GAA-FET and predicted its electrical characteristics by utilizing four different dielectrics i.e. HfO_2, Al_2O_3, Si_3N_4 and SiO_2. For this we have calibrated the simulator with experimental results using quantum models and solving Schrödinger equations in transverse direction where confinement occurs. Since Si-SiO_2 interface has better quality in fabrication process [2, 34], gate dielectric for all four devices under study is comprising of two layers of SiO_2 on silicon channel and a high-k dielectric on top of SiO_2.

The rest of this paper consists of three other sections. In section II we explain the device geometry and its parameters along with simulation considerations. Electrical characteristic results are discussed in section III. A comprehensive conclusion about this work is offered in section IV.

DEVICE PARAMETERS AND SIMULATION SETUP

Fig. 1 depicts a schematic view of GAA-FET device understudy. The cross section of this structure is circular. The silicon semiconductor channel has been covered by 0.5 nm silicon oxide and these two layers have been surrounded by 1nm high-k dielectric. This is due to better matching and interface quality of Si-SiO_2 which is formed in the fabrication process. All parameters of the physical and dimensional parameters related to this work are presented in Table 1.

Silvaco ATLAS simulator can predict the electrical characteristics of semiconductor devices at different bias conditions [35]. To have reliable results we first calibrated the simulator against experimental results from IBM as presented in [36], [37] and [23]. For this we estimated the 40.21 nm perimeter of silicon channel reported in [37] by a circle with radius of 6.4 nm and then fitted its electrical characteristics by setting conduction band effective mass and mobility for electrons. Fig.2(a,b) depict transfer characteristics (I_D-V_{GS}) and Gaussian like doping profile incorporated in the device for calibration at two low and high bias points corresponding to V_{DS}=0.05 V and V_{DS}=1.0 V, respectively.

In this work we enabled Schrodinger model to predict quantized density of states in the transverse direction (radius) for different orbital quantum numbers, where quantum mechanical

Table 1. Parameters of GAA-FETs under study.

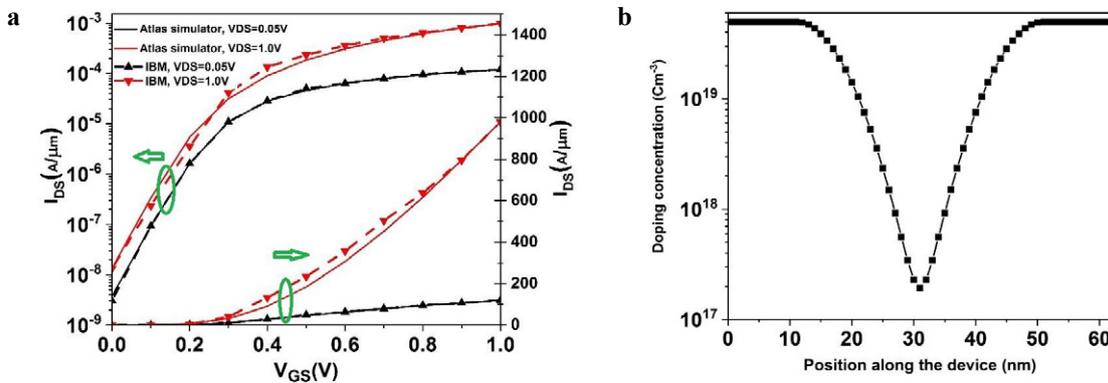| Parameter		Value
Gate oxide thickness	SiO$_2$ dielectric	0.5 nm
	High-k dielectric	1 nm
Circular silicon channel radius		6.4 nm
Channel Length (L$_G$)		22 nm
Source/Drain extended length (L$_S$/L$_D$)		20 nm
Gate Workfunction		4.512 eV
HfO$_2$ permittivity		22 [35]
Al$_2$O$_3$ permittivity		9.3[35]
Si$_3$N$_4$ permittivity		7.5[35]
SiO$_2$ permittivity		3.9[35]
Source/Drain doping		5*10^{19} cm^{-3}

Fig. 2. (a) Calibration of ATLAS simulator against IBM experimental results reported in [23, 36, 37] and (b) Gaussian doping profile considerations in calibration process.

confining potential variations occur. Solving self-consistent Schrödinger's and Poisson's equations can iteratively calculate carrier concentration (using eigen energies and wave functions) along with potential profiles and then the current in the device at each bias. Once carrier concentration is calculated, it is substituted in charge part of Poisson's equation. Then the potential extracted from Poisson's equation is substituted back into Schrödinger's equation. Alternating between Schrödinger's and Poisson's equations continues until a self-consistent convergence is obtained. We also enabled drift-diffusion mode-space (dd-ms) model. This is a semi-classical model to transport in devices with confinement in transverse direction and it has performed as an alternative to fully quantum non-equilibrium green's function (NEGF) model. However, the classical drift-diffusion equation is solved instead of quantum transport equation in this model. So, quantum effects in transverse direction is performed (by Schrödinger model), while all models related to mobility and

recombination can be inherited. It is worth noting that calculation and simulation time in dd-ms model is faster than NEGF [31].

It should be noted that the aim of this work is prediction and evaluation of the electrical characteristics of the calibrated GAA-FET with different high-k materials in terms of ON-current, OFF-current, subthreshold slope and transconductance.

RESULTS AND DISCUSSION

The transfer characteristics (I$_D$-V$_{GS}$) of the device under study with four different dielectrics has been shown in Fig. 3 at V$_{DS}$=0.05 V and V$_{DS}$=1.0V. According to this figure as the permittivity of gate dielectric increases drain current enhances and both OFF-current along with subthreshold slope (SS) are decreased. Therefore, GAA-FET with HfO$_2$gate dielectric seems much interesting for digital applications. This improvement in the device with higher permittivity dielectric is due to better electrostatic controllability of the gate over
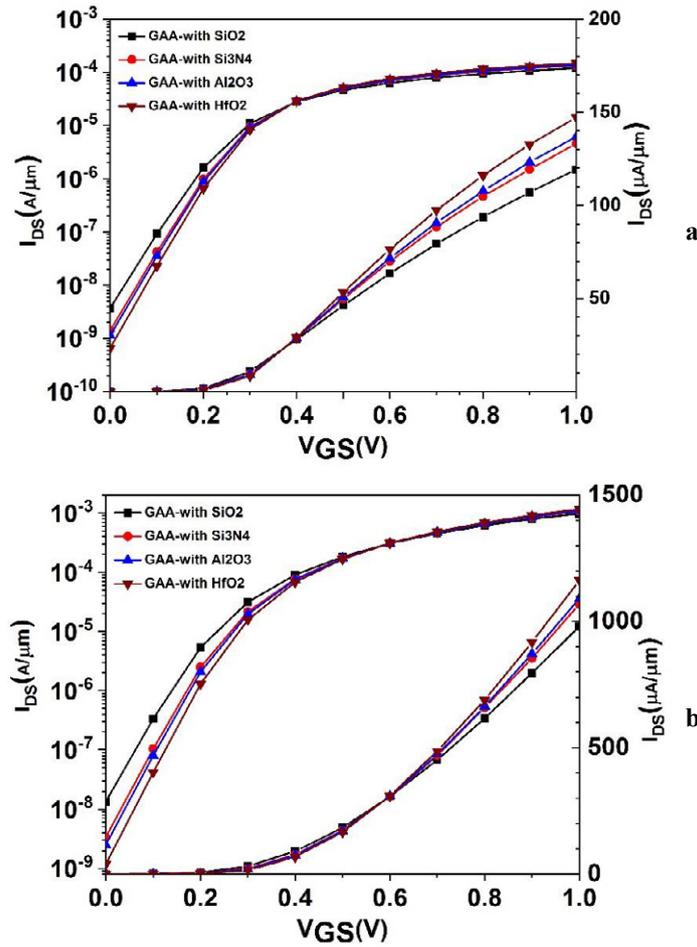
Fig. 3. Transfer characteristics of GAA-FET under study with different gate dielectric materials at (a) V_{DS}=0.05 V and (b) V_{DS}=1.0 V.

surrounded channel which intensively controls all of the carriers tending to pass from source to drain through the channel. Fig. 4 (a) depicts contour plot of electron concentration in the device at $V_{DS}=V_{GS}$=1.0 V for GAA-FET with HfO$_2$. Quantum confinement effect and receding electrons from Si-SiO$_2$ interface is obvious in this figure (a,b). First- three electron wave functions are presented in Fig. 4(c).Since squared wave function represent the electron occupation probability[33], electron concentration is expected to be lower in Si-SiO$_2$ interface. This is in agreement with achieved results of physical TCAD simulation as illustrated in Fig. 4(c). In fact, due to formation of a quantum well in Si-SiO$_2$ interface, electron energy will be quantized in transverse direction and electron

wave-like behavior will be dominant which results in a reduction of electron concentration at the interface.

Transconductance (g_m), shows how much the gate voltage influences on the drain current and is defined by following relation:

$$g_m = \frac{dI_D}{dV_{GS}}\bigg|_{V_{DS}=const} \tag{1}$$

This is an important parameter and shows amplification rate, somehow. Another parameter, g_m/I_D, reveals how much of energy dissipation (I_D), has led to amplification (g_m) in a device [2]. Based on this and Fig. 5 it is obvious that as the gate dielectric constant increases, g_m/I_D ratio will be enhanced and this improvement is higher at

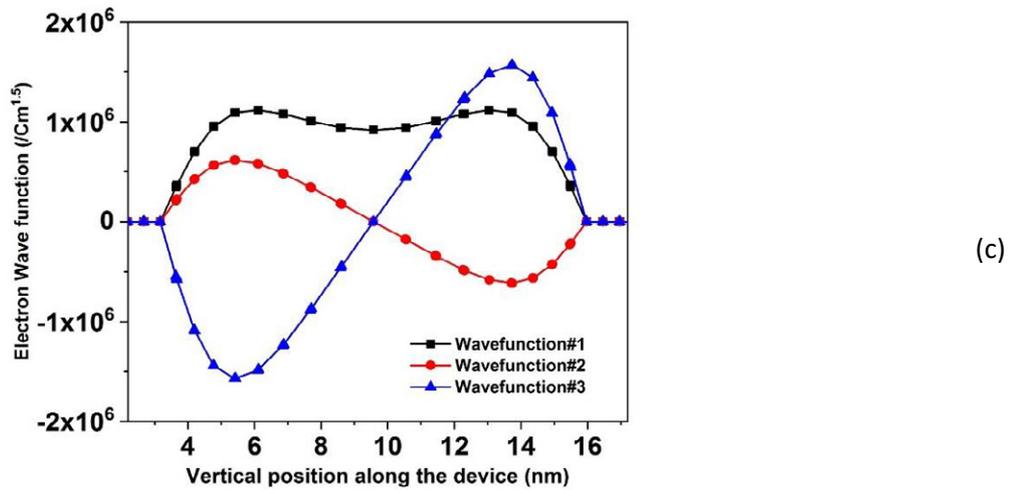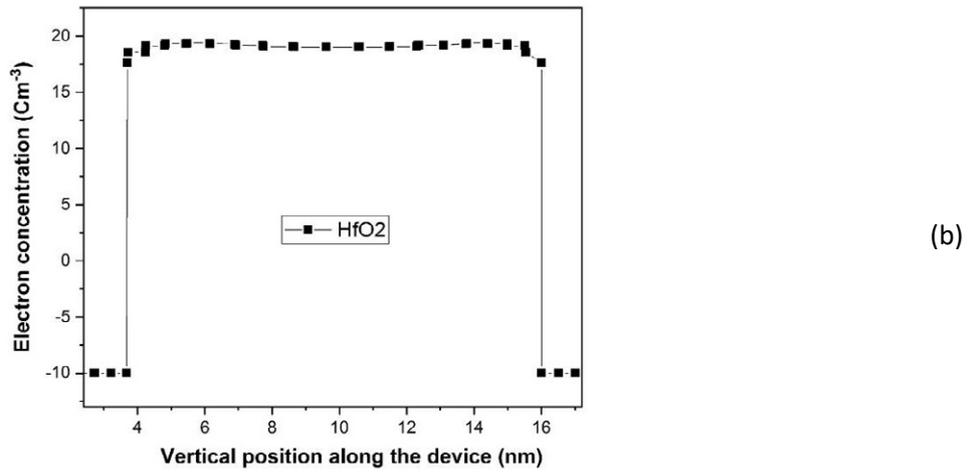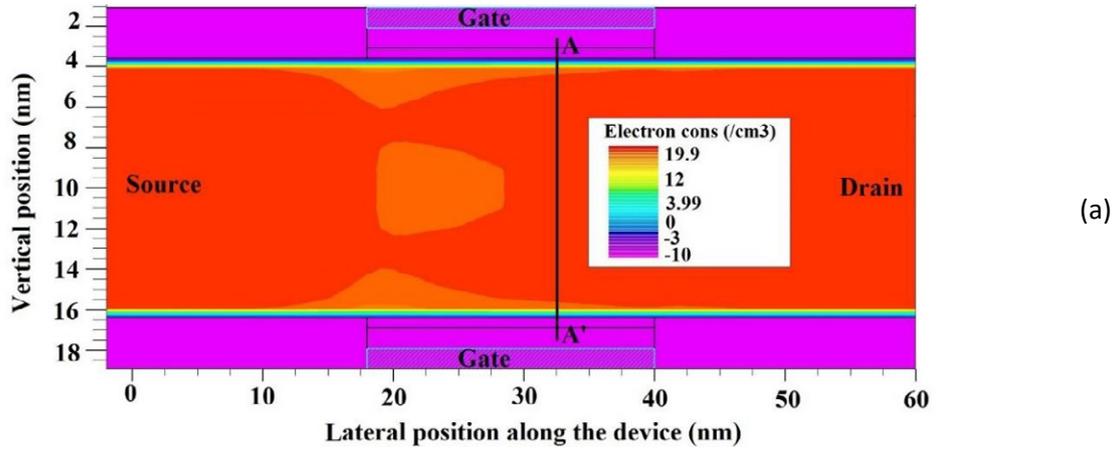Fig.4: (a) Electron concentration contour plot,(b)vertical electron concentration profile and (c)fist-three electron wave functions of GAA-FET with HfO$_2$ at bias V$_{DS}$=V$_{GS}$=1.0 V. Electron concentration and wave function in (b) and (c) have been given by a cutline from AA' segment in (a).
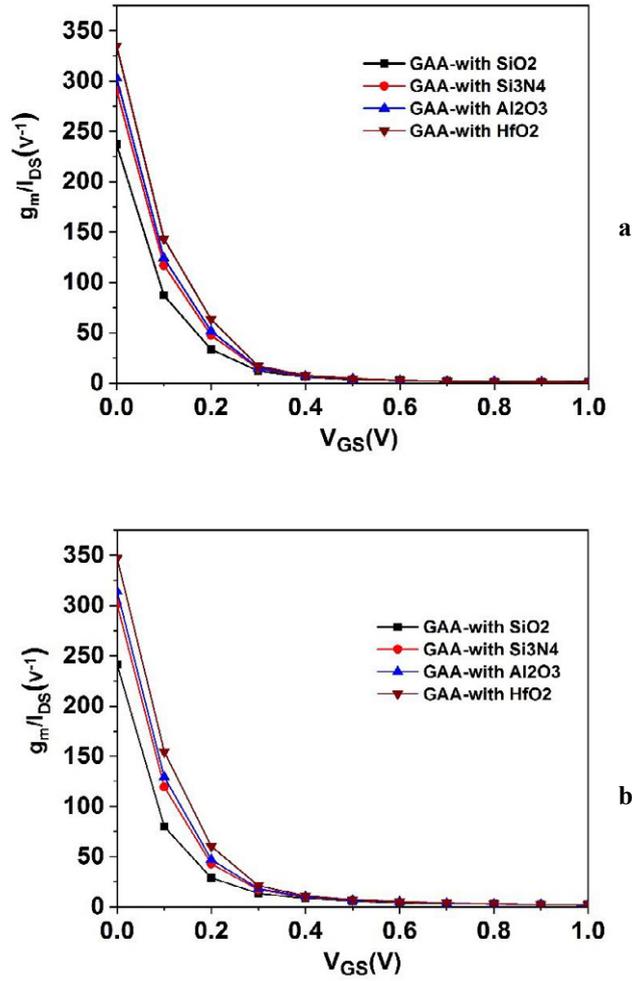
Fig. 5. Transconductance over drain current ratio of GAA-FET under study with different gate dielectric materials at (a) V_{DS}=0.05 V and (b) V_{DS}=1.0 V.
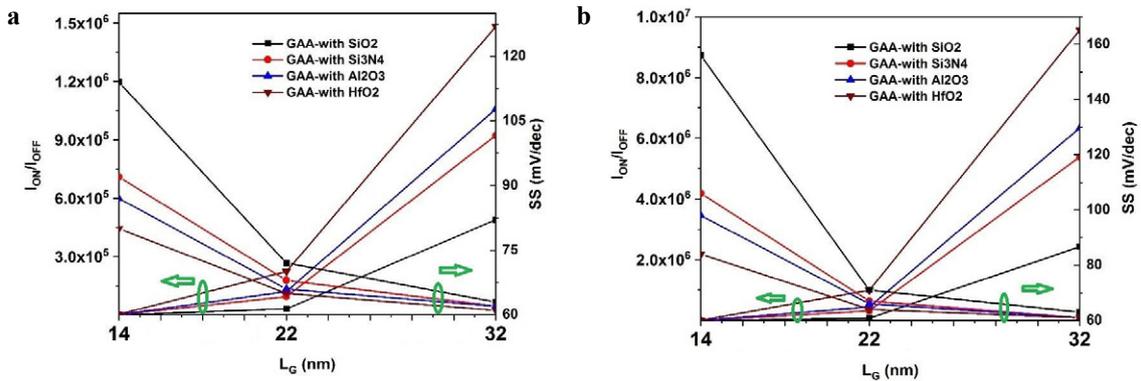

Fig. 6. I_{ON}/I_{OFF} ratio in left and SS in right versus channel length for GAA-FET under study with different gate dielectric materials at (a) V_{DS}=0.05 V and (b) V_{DS}=1.0 V.

lower gate voltages (V_{GS}). According to this figure, GAA-FET with HfO_2 dielectric has higher g_m/I_D ratio compared to other counterparts and it is because of better subthreshold region behavior in this device.

In another investigation, the channel length of GAA-FET with different high-k materials has been scaled down and then I_{ON}/I_{OFF} ratio along with SS for channel lengths of 32nm, 22nm and 14 nm were investigated. According to Fig. 6 by scaling, I_{ON}/I_{OFF} ratio is decreased while SS is increased for all device GAA-FET with different dielectrics, and the degradation amount for the device with lower permittivity is more. This is due to this reality that by scaling, the gate influence on the device performance particularly in subthreshold region reduces, which this can be partly compensated by using high-k dielectrics.

CONCLUSION

In this work we investigated the electrical characteristics of a GAA-FET with different high-k dielectric materials in the gate comprising of HfO_2, Al_2O_3, Si_3N_4 and SiO_2. It was shown that GAA-FET with HfO_2 dielectric has better performance in terms of I_{ON}, I_{OFF}, SS and g_m/I_D ratio. Our physical simulations also showed that both I_{ON}/I_{OFF} and SS parameters were degraded by scaling, and this is mostly related to subthreshold slope behavior degradation, where off-state current increases in the device. Based on our predictive simulation results, using high-k dielectric in the gate can improve the device electrical characteristics and it is seriously necessary for following Moore's low.

CONFLICT OF INTEREST

The authors declare that there is no conflict of interests regarding the publication of this manuscript.

REFERENCES

1. Karbalaei M, Dideban D. A novel Silicon on Insulator MOSFET with an embedded heat pass path and source side channel doping. Superlattices and Microstructures. 2016;90:53-67.
2. Colinge J-P. Silicon-on-Insulator Technology: Materials to VLSI. Springer US; 2004.
3. Weste NH, Harris D. CMOS VLSI design: a circuits and systems perspective. fourth ed: Pearson Education 2011.
4. Taur Y, Ning TH. Fundamentals of modern VLSI devices: Cambridge university press; 2013.
5. Orouji AA, Anvarifard MK. SOI MOSFET with an insulator region (IR-SOI): A novel device for reliable nanoscale CMOS circuits. Materials Science and Engineering: B.

2013;178(7):431-7.
6. Mehrad M, Ghadi ES. C-shape silicon window nano MOSFET for reducing the short channel effects. 2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS); 2017/04: IEEE; 2017.
7. Anvarifard MK, Orouji AA. Proper Electrostatic Modulation of Electric Field in a Reliable Nano-SOI With a Developed Channel. IEEE Transactions on Electron Devices. 2018;65(4):1653-7.
8. Schwierz F. Graphene transistors. Nature Nanotechnology. 2010;5(7):487-96.
9. Karbalaei M, Dideban D. A Scheme for Silicon on Insulator Field Effect Transistor with Improved Performance using Graphene. ECS Journal of Solid State Science and Technology. 2019;8(9):M85-M92.
10. Naderi A. Higher Current Ratio and Improved Ambipolar Behavior in Graphene Nanoribbon Field Effect Transistors by Symmetric Pocket Doping Profile. ECS Journal of Solid State Science and Technology. 2016;5(12):M148-M53.
11. Castro EV, Novoselov KS, Morozov SV, Peres NMR, dos Santos JMBL, Nilsson J, et al. Biased Bilayer Graphene: Semiconductor with a Gap Tunable by the Electric Field Effect. Physical Review Letters. 2007;99(21).
12. Nanmeni Bondja C, Geng Z, Granzner R, Pezoldt J, Schwierz F. Simulation of 50-nm Gate Graphene Nanoribbon Transistors. Electronics. 2016;5(4):3.
13. Yadav DS, Sharma D, Raad BR, Bajaj V. Dual workfunction hetero gate dielectric tunnel field-effect transistor performance analysis. 2016 International Conference on Advanced Communication Control and Computing Technologies (ICACCCT); 2016/05: IEEE; 2016.
14. Choi WY, Lee HK. Demonstration of hetero-gate-dielectric tunneling field-effect transistors (HG TFETs). Nano Convergence. 2016;3(1).
15. Dash S, Mishra GP. An extensive electrostatic analysis of dual material gate all around tunnel FET (DMGAA-TFET). Advances in Natural Sciences: Nanoscience and Nanotechnology. 2016;7(2):025012.
16. Mamidala JK, Vishnoi R, Pandey P. Tunnel Field-Effect Transistors (TFET). John Wiley & Sons, Ltd; 2016.
17. Mobarakeh MS, Moezi N, Vali M, Dideban D. A novel graphene tunnelling field effect transistor (GTFET) using bandgap engineering. Superlattices and Microstructures. 2016;100:1221-9.
18. Naderi A, Tahne BA. T-CNTFET with Gate-Drain Overlap and Two Different Gate Metals: A Novel Structure with Increased Saturation Current. ECS Journal of Solid State Science and Technology. 2016;5(8):M3032-M6.
19. Saurabh S, Kumar MJ. Fundamentals of Tunnel Field-Effect Transistors: CRC Press; 2016 2016/10/26.
20. Shaker A, El Sabbagh M, El-Banna MM. Influence of Drain Doping Engineering on the Ambipolar Conduction and High-Frequency Performance of TFETs. IEEE Transactions on Electron Devices. 2017;64(9):3541-7.
21. Naderi A, Ghodrati M. Cut Off Frequency Variation by Ambient Heating in Tunneling p-i-n CNTFETs. ECS Journal of Solid State Science and Technology. 2018;7(2):M6-M10.
22. Saremi M, Afzali-Kusha A, Mohammadi S. Ground plane fin-shaped field effect transistor (GP-FinFET): A FinFET for low leakage power circuits. Microelectronic Engineering. 2012;95:74-82.
23. Nagy D, Indalecio G, Garcia-Loureiro AJ, Elmessary MA,

Kalna K, Seoane N. FinFET Versus Gate-All-Around Nanowire FET: Performance, Scaling, and Variability. IEEE Journal of the Electron Devices Society. 2018;6:332-40.

24. Li M, Yeo KH, Suk SD, Yeoh YY, Kim D-W, Chung TY, et al., editors. Sub-10 nm gate-all-around CMOS nanowire transistors on bulk Si substrate. 2009 Symposium on VLSI Technology; 2009: IEEE.

25. Kumar P, Singh S, Singh NP, Modi B, Gupta N. Germanium v/s silicon Gate-all-around junctionless nanowire transistor. 2014 2nd International Conference on Devices, Circuits and Systems (ICDCS); 2014/03: IEEE; 2014.

26. Madan J, Chaujar R. Interfacial Charge Analysis of Heterogeneous Gate Dielectric-Gate All Around-Tunnel FET for Improved Device Reliability. IEEE Transactions on Device and Materials Reliability. 2016;16(2):227-34.

27. Lv Y, Qin W, Wang C, Liao L, Liu X. Recent Advances in Low-Dimensional Heterojunction-Based Tunnel Field Effect Transistors. Advanced Electronic Materials. 2018;5(1):1800569.

28. Bangsaruntip S, Cohen GM, Majumdar A, Zhang Y, Engelmann SU, Fuller NCM, et al. High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling. 2009 IEEE International Electron Devices Meeting (IEDM); 2009/12: IEEE; 2009.

29. Gaffar M, Alam MM, Mamun SA, Zaman MA, Bhuiya AK. A novel approach of modeling channel potential for Gate All Around nanowire transistor. TENCON 2010 - 2010 IEEE Region 10 Conference; 2010/11: IEEE; 2010.

30. Narang R, Saxena M, Gupta RS, Gupta M. Drain current model for a gate all around (GAA) p–n–p–n tunnel FET. Microelectronics Journal. 2013;44(6):479-88.

31. Association SI. International Technology Roadmap for Semiconductors, 2017.

32. Auth CP, Plummer JD. Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's. IEEE Electron Device Letters. 1997;18(2):74-6.

33. Hanson GW. Fundamentals of nanoelectronics: Pearson Education; 1 edition; 2011.

34. Bousari NB, Anvarifard MK, Haji-Nasiri S. Improving the electrical characteristics of nanoscale triple-gate junctionless FinFET using gate oxide engineering. AEU - International Journal of Electronics and Communications. 2019;108:226-34.

35. Atlas DS. Atlas user's manual. Silvaco International Software, Santa Clara, CA, USA. 2016.

36. Bangsaruntip S, Balakrishnan K, Cheng SL, Chang J, Brink M, Lauer I, et al. Density scaling with gate-all-around silicon nanowire MOSFETs for the 10 nm node and beyond. 2013 IEEE International Electron Devices Meeting; 2013/12: IEEE; 2013.

37. Elmessary MA, Nagy D, Aldegunde M, Seoane N, Indalecio G, Lindberg J, et al. Scaling/LER study of Si GAA nanowire FET using 3D finite element Monte Carlo simulations. Solid-State Electronics. 2017;128:17-24.