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RESEARCH PAPER

Improvement of a Nano-scale Silicon on Insulator Field Effect Transistor Performance using Electrode, Doping and Buried Oxide Engineering

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ABSTRACT

In this work, a novel Silicon on Insulator (SOI) MOSFET is proposed and investigated. The drain and source electrode structures are optimized to enhance ON-current while global device temperature and hot carrier injection are decreased. In addition, to create an effective heat passage from channel to outside of the device, a silicon region has embedded in the buried oxide. In order to reduce the device leakage current and controlling the threshold voltage, a p-type retrograde doping is introduced into channel region. Since the air has the least permittivity among materials, it can be utilized to decrease the device parasitic capacitances. Based on this, an air gap is embedded in the buried oxide near the silicon to improve RF performance of the device. Because the source and drain electrodes are embedded in and over the silicon film in the source and drain regions, we called this structure EEIOS-SOI MOSFET. "EEIOS" stands for "Embedded Electrodes In and Over the Silicon film". During this work, EEIOS-SOI MOSFET is compared with a conventional SOI MOSFET and another SOI MOSFET with just Embedded Electrodes In the Silicon Film (EEIS-SOI). EEIS-SOI presents better electrical figure of merits including lower subthreshold slope and lower leakage current in simulations. An immense investigation among these devices shows that EEIOS-SOI MOSFET has better transconductance, lower gate injection leakage current and lower temperature related to DC parameters and higher cut off frequency, gain bandwidth product and unilateral power gain related to AC figures of merits compared to its counterparts.

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INTRODUCTION

As silicon on insulator devices are surrounded by silicon dioxide (SiO_2) in the buries oxide (BOX), these devices suffer from self-heating effect (SHE) phenomenon [1]. Because SiO_2 has lower thermal conductivity compared to silicon [2]. SHE in a device is detrimental and will reduce carrier saturation velocity and mobility and it may be resulted in reduced reliability [3-5]. Moreover, by continuous scaling and increasing the number of transistors in the chip short channel effects (SCE) increase [6-10], and power density is passing from sun power density per unit area [11]. So in this case, it is necessary to make a difference and

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reduce power dissipation.

Different analytical models have been studied to consider the SOI MOSFETs for the accurate modeling [12-14], and recently, the authors in the literatures [15-21] proposed interesting SOI structures by modifying the silicon film and BOX layers structure which result in SCE and SHE improvement. In this work, the effect of source/drain electrode geometriesof SOI-MOSFETs have been considered and optimized to improve the electrical characteristics in these devices, what is not reported earlier. A silicon region has embedded in the buried oxide to reduce device temperature. In order to our proposed device with embedded electrode in and over the silicon film (EEIOS-SOI) has better DC and AC performance, an air region with k=1 [22] close to silicon in the BOX and a heavily p-type retrograde doping underneath the channel are applied. Air with dielectric constant of k=1 can improve RF gains. Embedding heavily p-type retrograde doping, sets threshold voltage, blocks carrier transition in the depth of the channel by scattering the carriers and then reduces off current. In the following, all improvements are explored in comparison with a conventional SOI structure (C-SOI) and another SOI MOSFET with embedded electrode in the silicon film (EEIS-SOI) at which this device had shown good characteristics in optimization steps.

The remaining of this work is divided into three sections. In the section two, source and drain electrodes geometry is selected and device parameters are introduced. In section three, the simulated and extracted results in terms of ac and dc electrical performance are illustrated. In the last section, we explain comprehensive conclusion for the presented study.

EEIOS-SOI DEVICE DESIGN

For selecting the best electrode geometry in the source and drain of SOI MOSFET with device dimensions determined in the table 1, we considered sixteen different cases. Fig. 1(a-n) illustrates a cross-section view of these considered cases. At first, for just considering the effect of electrode geometries on the device electrical characteristics, we didn't inserted retrograde doping, silicon and air regions in the device. Our figure of merits in the first step were selecting devices with highest on current, highest transconductance, lowest off current and subthreshold slope. Among these devices Fig. 1(b) structure had the lowest off current and subthreshold slope and Fig. 1(j) had the highest on current and transconductance. By considering Fig. 1(a) as a conventional structure, in the second step we added retrograde doping, silicon and air regions to the selected structures i.e. Fig. 1(b,j) to have more comprehensive investigation in this paper. Fig. 2(a-c) shows the schematic view of three structures which is investigated in the following. Fig. 2(a) is the conventional (C-SOI) structure and Fig. 2(b) and (c) are EEIS-SOI and EEIOS-SOI structures respectively, which their appellation pointed before. It should be noted we added embedded silicon region exactly underneath of the channel with the most temperature i.e. close to drain region where impact ionization and collision occurs. Our simulations showed addition an air region beside this silicon region in the BOX

Table 1. Parameters for C-SOI, EEIS-SOI and EEIOS-SOI structures.

Parameter	Values		
	C-SOI	EEIS-SOI	EEIOS-SOI
Top oxide thickness (Tox)	0.5 nm	0.5 nm	0.5 nm
Silicon channel thickness	9 nm	9 nm	9 nm
Buried oxide thickness (BOX)	41 nm	41 nm	41 nm
Retrograde doping thickness	-	7 nm	7 nm
Embedded silicon/air region thickness in the BOX	-	30 nm	30 nm
Channel Length	15 nm	15 nm	15 nm
Source/Drain Extension Length	10 nm	10 nm	10 nm
Source/Drain Electrode Length in and over the silicon film	9 nm	9 nm	9 nm
Retrograde doping length	-	9 nm	9 nm
Embedded silicon region length in the BOX	-	6 nm	6 nm
Embedded air region length in the BOX	-	7 nm	7 nm
Gate Workfunction	4.6 eV	4.6 eV	4.6 eV
Channel/substrate doping (p-type)	1e12 cm^{-3}	1e12 cm^{-3}	1e12 cm^{-3}
Source/Drain doping (n-type)	9e18 cm^{-3}	9e18 cm^{-3}	9e18 cm^{-3}
Retrograde doping	-	2e19 cm^{-3}	2e19 cm^{-3}

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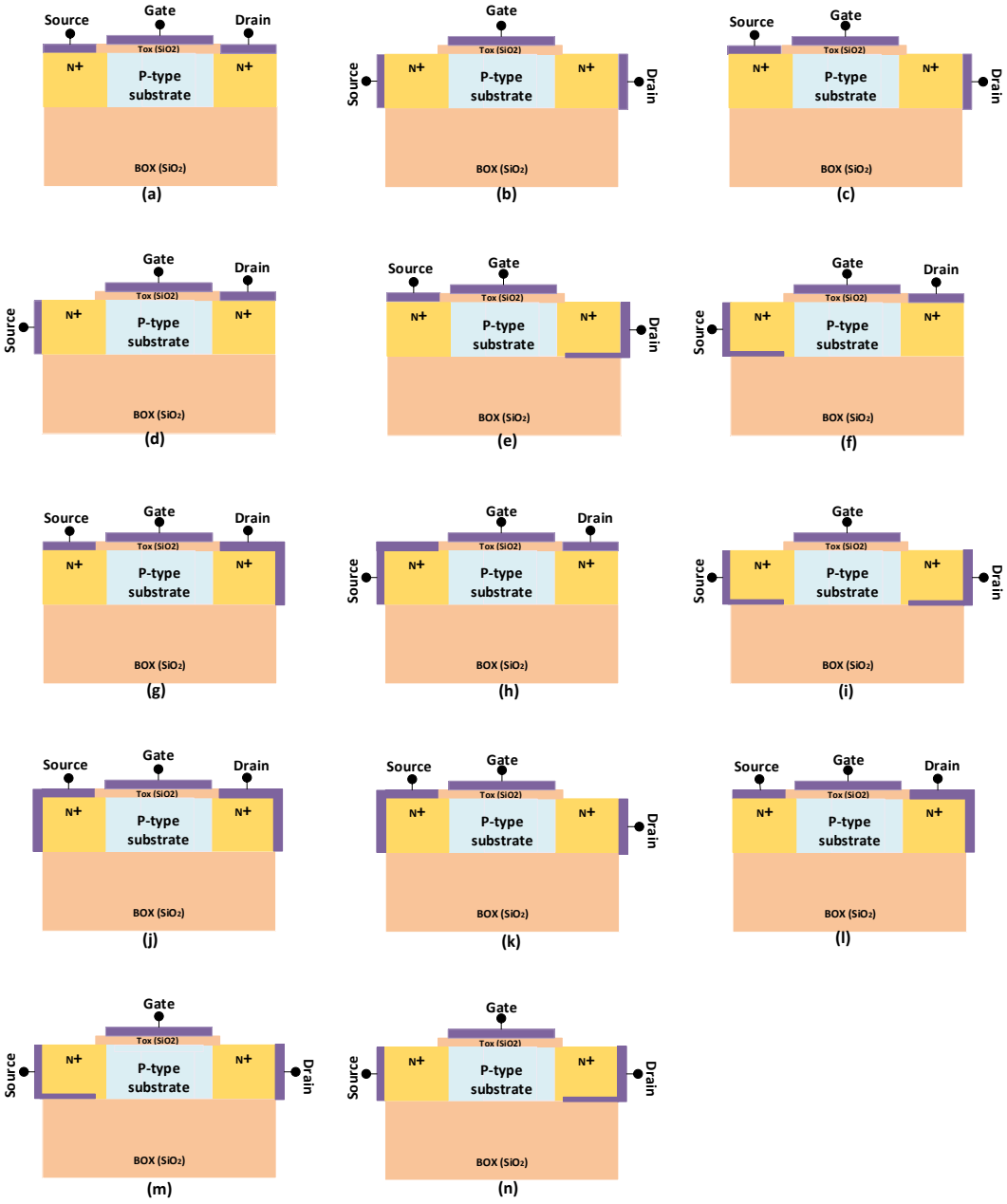

Fig. 1. Different source and drain electrodes geometry considered in this research.

can improve RF characteristics proportionally in comparison to silicon or SiO_2 in the box at the same place. The complete device parameters related to these devices presents in the table 1.

To examine the different electrical characteristics of theproposed SOI device, 2-D ATLAS device simulator was used. In order to have reliable results, we used FermiDirac distribution function in the device. We used both SRH and Auger models to enable generation/recombination like [2, 23]. FLDMOB and CONMOB models were added to consider field and concentration dependent mobility. HEI and HHI were added to take into account hot electron and hole injection in the gate. HCTE and LAT.TEMP models were also included to considerelectron temperature in

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transport model and global device temperature. BGN model accounted for applying temperature and doping dependence of the band gap,and IMAPC SELB capability modeled impact ionization in simulations [24].

RESULTS AND DISCUSSION

In this section we discuss about the reliability of the EEIOS-SOI in terms of both dc and ac electrical performances, comprehensively.

DC-state electrical performances

In VLSI, we explore transistors which they have low off current, high on current, low subthreshold slope and threshold voltage close to half of supply voltage [11, 25]. Fig. 3(a) and (b) shows the linear and semi logarithmic transfer characteristics of three considered MOSFETs at V_{DS}=0.8 V, respectively. According to this figure, it is obvious that EEIS-SOI and EEIOS–SOI MOSFETs can satisfy the abovementioned items in the same

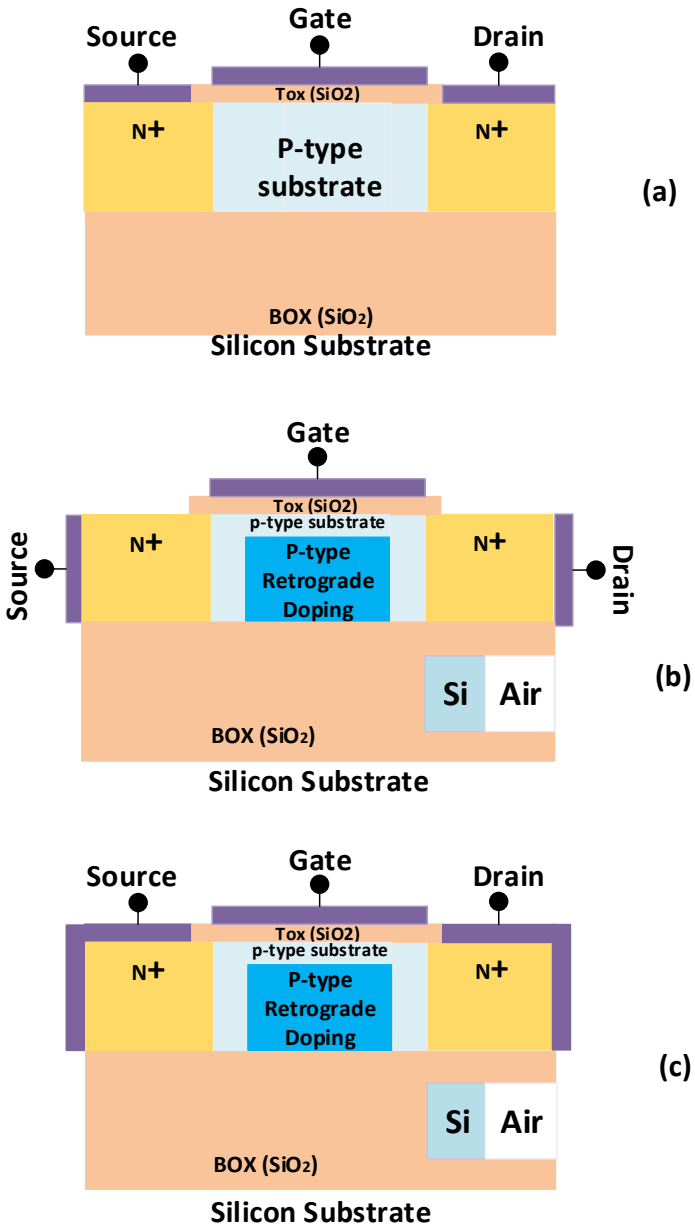

Fig. 2. Cross section view of: (a) C-SOI, (b) EEIS-SOI and (c) EEIOS-SOI structures.

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device parameters according to table 1. Low off current and subthreshold slope of S=67 mV/dec in EEIS-SOI and EEIOS-SOI MOSFETs are indicator of insignificant static power dissipation and high speed in switching from OFF-state to ON-state, respectively. Although C-SOI MOSFET has high drive current, but leakage current in this device is very high and it is not in line with our desires. Due to the drive current of 1.3 mA and threshold voltage close to the half of V_{GS}=0.9 V, EEIOS-SOI structure i.e. engineered structure of C-SOI, is an excellent transistor which is according to ITRS requests [26]. This figure shows by truly engineering the C-SOI structure, devices with better characteristics are still achievable.

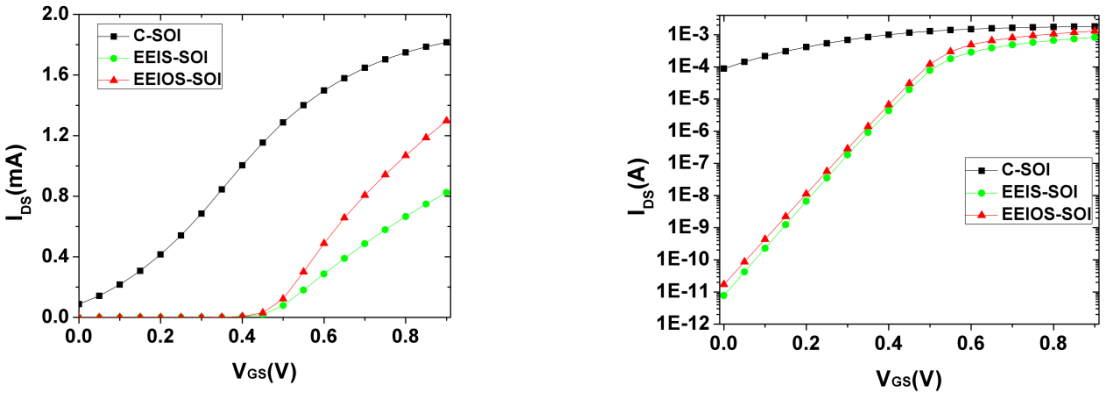
Ideally, a MOSFET in which its drain current is controlled by gate-source voltage, is a good one. Transconductance is a measure to consider this and it is very important parameter because it influences on drive current and RF gains and parameters [27, 28]. Transconductance is defined by the following relation [29]:

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{V_{DS}=const} \quad (1)$$

Which I_D, V_{GS} and V_{DS} are drain current, gate-source voltage and drain-source voltage, respectively. From Fig. 4, it is clear that g_m in EEIS-SOI and EEIOS-SOI MOSFETs are zero at subthreshold voltages and it suddenly increases after threshold voltage. Transconductance amount, g_m, is higher in EEIOS-SOI MOSFET after threshold voltage which this is indicator of better gate controllability over drain current in this device compared to its counterparts.

In short channel MOSFETs, when carriers pass through the channel, because they achieve high energy from the drain-source electric field they collide to atoms near the drain and hot carriers exist [25]. Because this carriers are energetic, they can tunnel to the gate and cause gate leakage current or enter to drain terminal. This is an unwanted phenomenon because passage of carriers through the gate can damage the gate oxide and change threshold voltage by the time [11]. According to the Fig. 5 (a), gate hot electron current in EEIOS-SOI is lower than its counterparts and then it is more reliable and C-SOI MOSFET is more impressed by this hot carriers. Fig. 5(b) depicts drain hot electron current. Drain hot electron current in EEIOS-SOI is more than EEIS-SOI. This means hot carriers in EEIOS-SOI MOSFET after existence are mostly absorbed by lateral drain electrode and fewer electrons tend to tunnel to the gate electrode. So the lateral electrode in drain of EEIOS-SOI helps it to enhance its reliability against this short channel phenomenon. It is obvious C-SOI MOSFET has a weak reaction against hot carriers.

Device temperature in SOI MOSFETs is a serious problem, as the device is surrounded by insulator and there is not easy path for heat to pass from. Fig .6 presents global device temperature of three MOSFETs. It is clear that EEIOS-SOI MOSFET has much lower temperature in comparison to its counterparts at all drain voltages. This good happening is indebted to both embedded silicon region in BOX and electrode structure in EEIOS-SOI. Lateral electrodes in EEIOS-SOI cause electrons spend lower path along the device and



(a) (b)

Fig. 3. Transfer characteristics (ID-VGS) for C-SOI, EEIS-SOI and EEIOS-SOI MOSFETs at VDS=0.8V: (a) linear view (b) semi logarithmic view.

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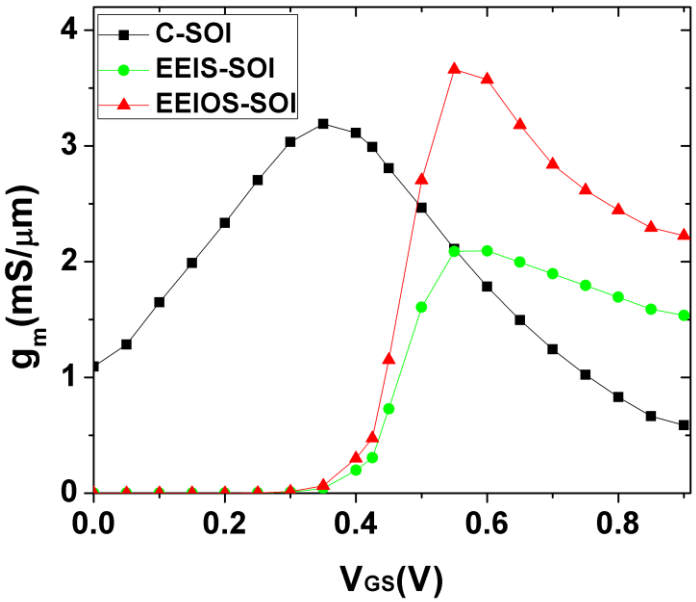

Fig. 4. Transconductance in for C-SOI, EEIS-SOI and EEIOS-SOI MOSFETs at VDS=0.8V.

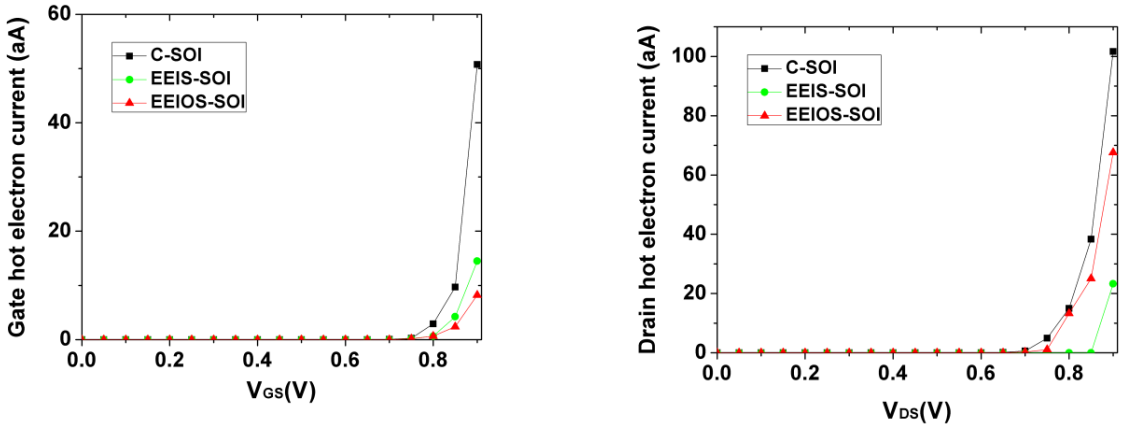

Fig. 5. (a) Gate hot electron current at VDS=0.8 V, (b)Drain hot electron current at VDS=0.9 V for C-SOI, EEIS-SOI and EEIOS-SOI MOSFETs at VGS=0.9V.

second it participate in device heats. According to the following relation [3]:

$$\mu_{eff} = \mu_{effo,0}\left(\frac{T}{T0}\right)^{-K} \quad (2)$$

In this relation T, $T_0$and $\mu_{effo,0}$are channel temperature, ambient temperature and effective mobility in ambient respectively. K is the mobility temperature exponent which has a typical value in range of 1.5-1.7 for n-channel transistors [30]. Based on above relation, device temperature leads to mobility degradation and then drain current reduction. So it is very important to keep the device temperature low enough to increase its abilities.

Fig. 7 depicts output characteristics of C-SOI, EEIS-SOI and EEIOS-SOI MOSFETs. According to this figure, although C-SOI MOSFET has significant drive current, but it has a negative slope in high drain-source voltages in saturation region. This is because of mobility degradation due to self-heating phenomenon [15]. In fact, based on relation (2) by increasing the device temperature, electrons mobility reduce and this leads to drain current reduction and immense its reliability. According to this figure EEIOS-SOI MOSFET

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has higher drive current compared to EEIS-SOI MOSFET, due carriers pass shorter pass along the device and then absorbed by drain terminal. So this device can as well be excellent in analogue application.

AC-state electrical performances

In the following we investigate RF performance of C-SOI, EEIS-SOI and EEIOS-SOI in terms of cut off frequency, gain bandwidth production (GBP) and unilateral power gain which they are of important figures of merit in RF applications.Cutoff frequency, corresponds to frequency at which the small-signal current gain is equal to unity[1, 28]. The cutoff frequency is given by the following expressions:

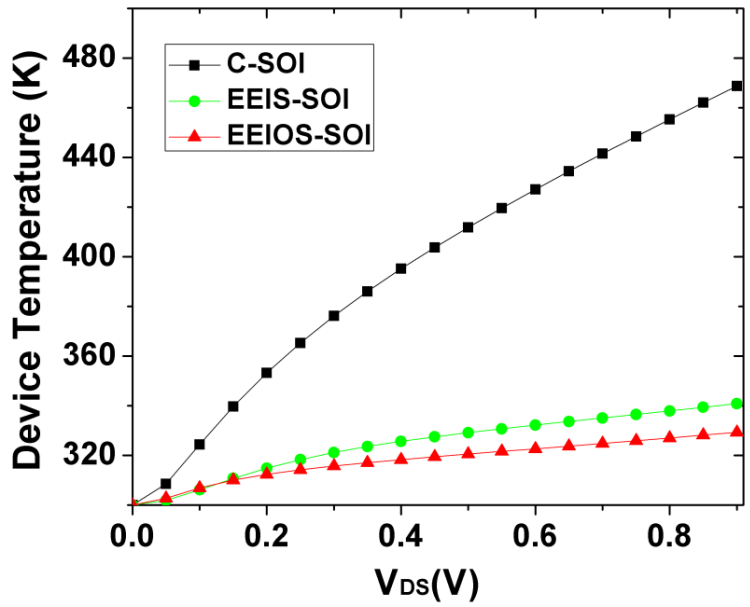

Fig. 6. Global device temperature in C-SOI, EEIS-SOI and EEIOS-SOI MOSFETs at VGS=0.9V.

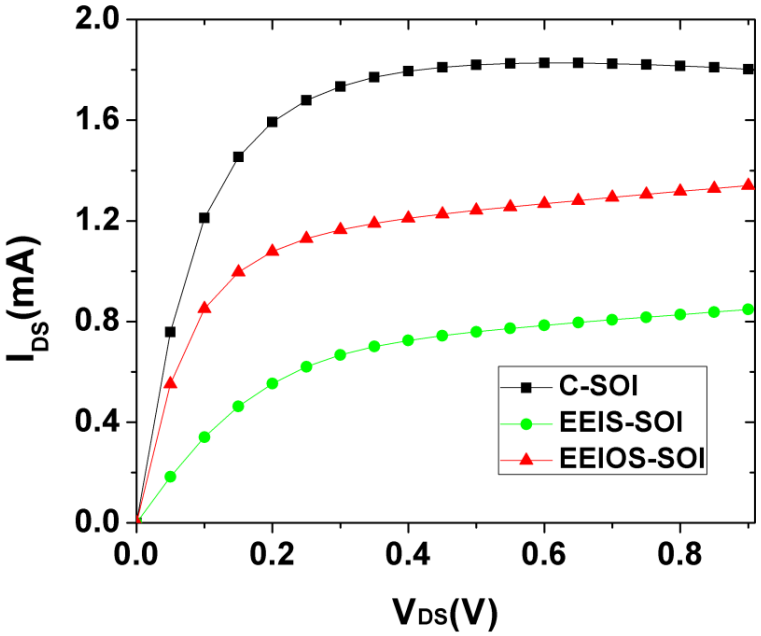

Fig. 7. Output characteristics of C-SOI, EEIS-SOI and EEIOS-SOI MOSFETs at VGS=0.9V.

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$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (3)$$

Where g_m, C_{gs} and C_{gd} are transconductance, gate-source and gate-drain capacitances, respectively. From Fig. 8, it is clear that after threshold voltage when transistor is ON-state, EEIOS-SOI MOSFET has highest cutoff frequency compared to other counterparts. Because graphs in this figure are formed like graphs of g_m in Fig. 4, so this enhancement is certainly indebted to higher g_m values in EEIOS-SOI MOSFET.

Gain bandwidth product (GBP) is also a figure of merit which is calculated as [28]:

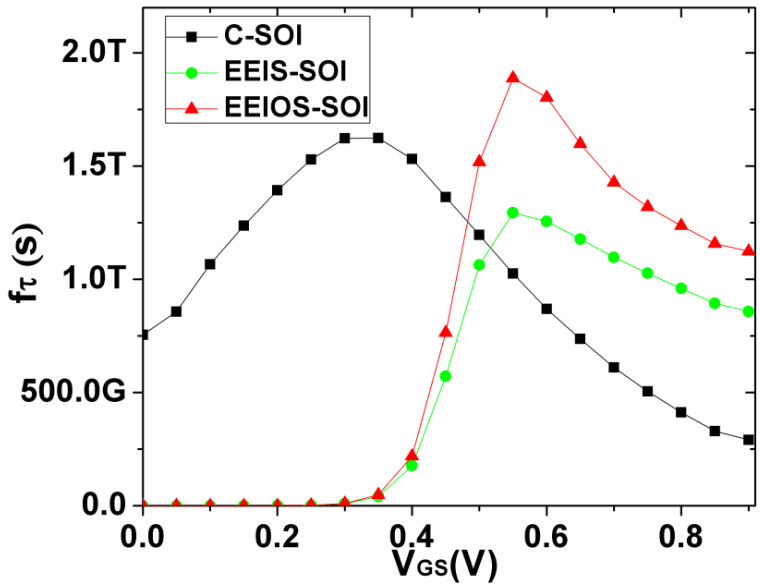

Fig. 8. Cutoff frequency as a function of gate-source voltage for C-SOI, EEIS-SOI and EEIOS-SOI at bias VDS =0.8 V and f=1MHz.

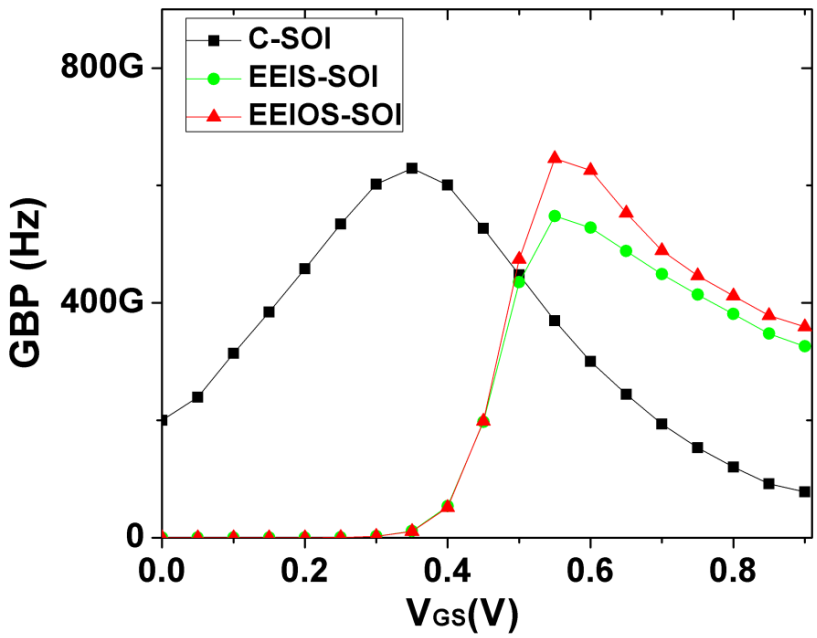

Fig. 9. Gain bandwidth product (GBP) as a function of gate-source voltage for C-SOI, EEIS-SOI and EEIOS-SOI at bias VDS =0.8 V and f=1MHz.

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$$GBP = \frac{g_m}{(20\pi * C_{gd})} \quad (4)$$

Where g_m and C_{gd} are transconductance and gate-drain capacitance. According to the Fig. 9,EEIOS-SOI has higher GBP compared to its counterparts and this improvement is indebted to the higher g_m in this device with the same description which pointed for cutoff frequency improvement.

Fig. 10 depicts unilateralpower gain as function of frequency. This gain is a figure of merits in RF applications too. From this figure two excellence can be obtained for EIOS-SOI MOSFET. First EIOS-SOI MOSFET has higher unilateral power gain. Second, due to the graph intercept point to the frequency axis in this figure determines maximum oscillation frequency (f_{max}) [1], so EIOS-SOI device has higher oscillation frequency. The maximum oscillation frequency, f_{max}, is the frequency at which the small-signal power gain is equal to unity under optimum matching conditions [1]. According to these results EEIOS-SOI is excellent for RF application compared with its counterparts.

CONCLUSION

In this work we investigated the dc and ac states performance of EEIOS-SOI and EEIS-SOI and C-SOI MOSFETs. In EEIOS-SOI structure due to both special drain and source electrodes and embedded silicon region in the buried oxide (BOX), global device temperature improved. Embedded electrodes in and over the silicon film help carriers pass shorter length and be absorbed by electrodes more effectively compared to EEIS-SOI MOSFET and helps in lattice temperature reduction. Embedded silicon region due to having higher thermal conductivity compared to SiO_2, conducts heats more effectively out of device. Because EEIOS-SOI was cooler compared to its counterparts, so electrons had higher mobility in it and then higher drain current and transconductance were the results. Because EEIOS-SOI MOSFET had high transconductance, this device presented higher cutoff and maximum oscillation frequencies and gain bandwidth product, compared to other devices under study. Moreover, due to the fact that EEIOS-SOI showed acceptable merits comprised of low off current, low subthreshold slope, high reliability against hot carrier injection, threshold voltage value of half a supply voltage and higher unilateral power gain, this device seems interesting for VLSI integrated circuits.

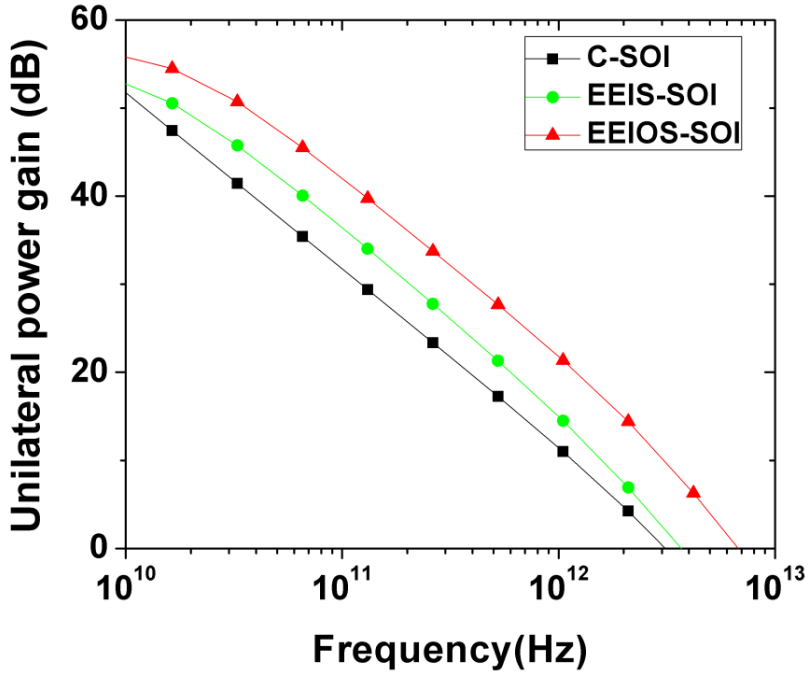

Fig. 10. Unilateral power gain as a function of frequency for the C-SOI, EEIS-SOI and EEIOS-SOI at bias VGS=0.9 V andVDS =0.8 V.

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CONFLICT OF INTERESTS

The authors declare that there is no conflict of interests regarding the publication of this paper.

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