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RESEARCH PAPER

Fabrication of 100nm Nano Pillars on Silicon

*Ujwala. A. Kshirsagar *,Mrinal Bachute*

Department of Electronics and Telecommunication Engineering, Symbiosis Institute of Technology, Pune, India

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ABSTRACT

The main objective of the project was to fabricate a vertical Gate All Around (GAA) p-i-n doped Tunneling Field Effect Transistor (TFET) device for which obtaining precise nanopillar structure was needed, to be optimized and achieved. This paper specifically focused on fabrication of Nano pillars on Silicon wafer using Hydrogen Silsesquioxane (HSQ). Initially we experimented with two methods Plasma Asher and AMAT Etch chamber. We have chosen HSQ resist for patterning high-resolution 100 nm circular dot structures for the fabrication of densely packed suspended vertical Si Nano pillars. This provides high etching resistivity of HSQ and better convenience of pattern transfer and selectivity from resist to various materials. In addition, epitaxial semiconductor Si wafers with different semiconductor layers have been directly implemented to render nanopillars with self-aligned and well-defined homo or hetero junction properties. These structures may be used to analyze evidence of the primary design of devices such as vertical surround Gate field effect transistors.

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INTRODUCTION

The continuous CMOS device scaling is suffering from short channel effects, increased Off-state leakage current and non-scalability of the operating supply voltage (Vdd). All these factors are compelling for different geometry transistors. GATE-ALL AROUND (GAA) or wrap around gate nanowire Compared to other gate designs such as double or tri-gated transistors, Field Effect Transistors (FET) have attracted a lot of attention for better electrostatic control [1]–[5]. To build up a cognitive computing system that will closely emulate biological neuron structure, present CMOS transistor should be modelled as low energy switching devices with high scalability. Therefore, we propose to fabricate a vertical wrap around nano-wire p-type Tunnel FET on the Si substrate. To fabricate such an ultrashort channel vertical nano-wire TFET devices of minimum footprint, without suffering thermal budget limit and serious short-channel effect (SCEs), was the main goal of the proposed structure. In addition, epitaxial grown semiconductor Si wafers with various semiconductor layers can be implemented directly to make nanopillar with homo or hetero junction properties that are self-aligned and well-defined. Such structures may be used to examine evidence of the principal architecture of devices such as the transistors for vertical surround Gate field effect [6]. EBL is difficult to apply to the fabrication of the silicon nanopillar array with large area [7]. Basically, the proposed vertical GAA nanowire p-TFET would include dominant fabrication stages like one of the prominent stages

* *Corresponding Author Email: ujwala.kshirsagar@sitpune.edu.in*

is Silicon nanowire array fabrication by applying Proximity effect correction (PEC), thereby Electron beam lithography and finally Reactive ion etching (RIE) using Hydrogen Silsesquioxane (HSQ) hard mask. This paper presents optimization recipe for Electron beam lithography (EBL) patterning of 100nm dots on HSQ resist.

The class of inorganic compounds with the chemical formula [HSiO3/2] * n is Hydrogen Silsesquioxane (HSQ). HSQ is an e-beam resistant negative-acting material that works well. It's not a normal resist, because it's not an organic polymer, it's a spin-on-glass material that after production actually leaves behind a SiO2 material in exposed are as It is often referred to by the old trade name FOX (which was short for Flowable Oxide). It is marketed by DOW CORNING as XR-1541 now. A significant role in the achievable resolution has been stated to be the thickness of the coated resist. It is immune to very high resolution, but needs a high dose, and so exposure is slower with Silsesquioxane with hydrogen (R = H). For the patterning and generation of semiconductor nanostructures, a low-cost Nano sphere lithography approach offers a possible alternative to traditional top-down manufacturing techniques [8]. The initial nanoparticle mask can regulate the shape and density of the nanopillar, which can be controlled by adjusting the initial film thickness and temperature of the annealing process. The silica nanopillar displays lower reflectance due to the moth-eye effect [9]. In a number of fields such as photonics and nano photonics [10-11], vertical nanostructures having aspect ratios greater than 1 are important.

Y. Guerfi et al., demonstrated with the top-down manufacturing of ultra-high density vertical silicon nanowire networks, 100 percent yield, and precise control of both diameter and position. First, e-beam lithography has been modelled dense and well-defined Nano pillar networks using a negative tone e-beam resistant Hydrogen Sylses Quioxane (HSQ) [12]. Though there are lots many techniques suggested and implemented we opt novelty in optimizing fabrication techniques for implementing Nanopillar which provides good selectivity for patterning material and improving the process of etching to remove HSQ after post processing. In our experiment, we have chosen top - down approach with HSQ resist for patterning high-resolution 100 nm circular dot structures for the fabrication of densely packed suspended vertical Si nano pillars due to the high etch resistance of HSQ and the selectivity freedom of transfer of pattern from resist to various material.

MATERIALS AND METHODS

Critical issues that occur during the manufacture by e-beam lithography of high-density nanostructures were considered by Jung-Sub Wi et al. They made a 25-nm-pitch Si nanopillar array and a 15-nm-pitch nanodot resist array [13]. In combination with e-beam lithography, etching of the HSQ resist residues shows excellent flexibility, anisotropy, and selectivity of the process [14]. A circular dot pattern of Feature size 100nm successfully written by us on Materials like silicon, silicon nitride and silicon dioxide using HSQ negative resist by optimizing EBL parameters to 20kV (Electric High Tension) EHT, 7.5 µm aperture within dose factor window of 360 µC to 520 µC. Silicon oxide (SiOx) had also shown excellent efficiency of resistance switching [15]. The best results were found for plain Silicon sample.

We have used DOW Corning's XR-1541-006 E Beam resist in MIBK, a 6% dilution, for our

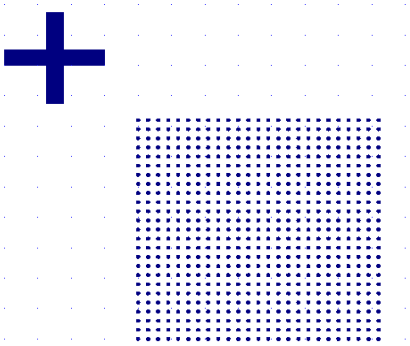


Fig. 1. Mask design used for patterning

experiment. The details of steps executed for experiment is listed below:

i) For Si wafer cleaning sample was dipped in acetone and then in isopropyl alcohol (IPA) for few second sample was dried using low pressure nitrogen gun.

ii) Cleaned Si sample was baked on hotplate for 15 min at 170 C for dehydration. Sample was being spin coated with 6% HSQ using 4000 rpm and 2000 rpm for 45 minutes after which was kept at 250 Celsius for 2 minutes.

iii) Patterning of 30x30 µm solid squares with an array of 25 x 25 of 100nm circular dots with a pitch of 300 nm as shown in following Fig. 1.

vi) Finally, sample was exposed to 20Kv Electric High Tension (EHT) with 60 µm Aperture for solid squares and 7.5µm Aperture for circular dots. Developed in 25% TMAH cold solution for 1-5 seconds and rinse in flowing distilled water for 30 sec. Developed sample was sent to take scanning electron microscope (SEM) Images.

Above process was successfully implemented

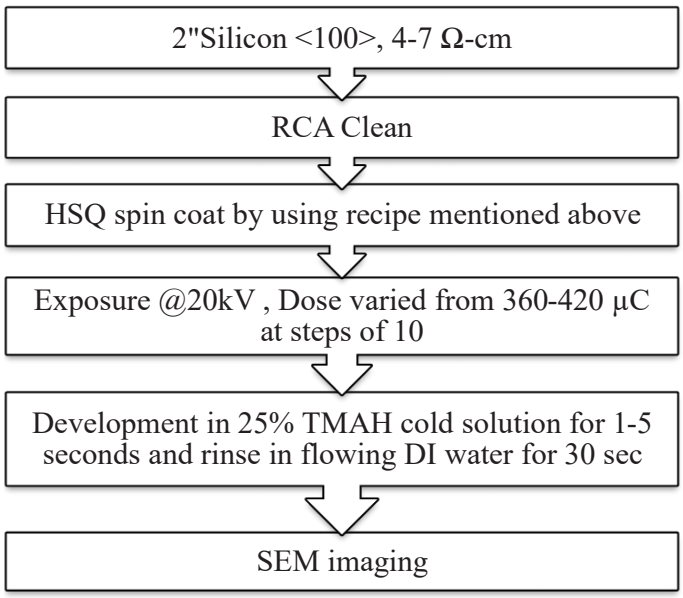


Fig. 2. Process Flow

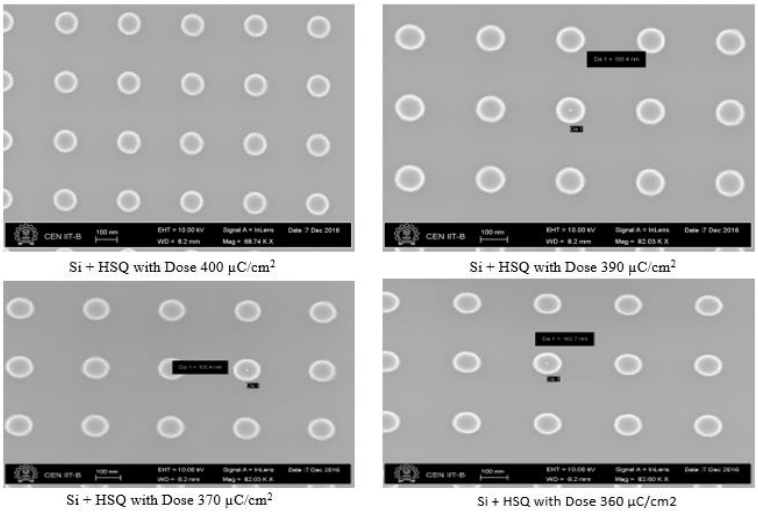


Fig. 3. circular dot pattern of feature size 100nm within dose factor window of 360 µC to 520 µC

for Silicon Nitride and Silicon Dioxide Sample. In case of both, the dose factor window for HSQ found out to be 320 µC- 520 µC. After the lift-off phase, gold (Au) Nano meshes with customizable nanostructures were achieved. Because of the aperiodic structures of disordered apertures, Au Nanomesh exhibited strong optoelectronic properties and non-iridescence without angle dependence [16]. Patterns below 320 µC dose were not coming good. Hence Nano pillars were developed with Plain Silicon wafer. Following Fig. 2 shows process flow for development of nano pillars on Si wafer

Following Fig. 3 shows results of a circular dot pattern of feature size 100nm and concluded that it can be successfully written on materials like silicon, using HSQ negative resist by optimizing EBL parameters to 20kV EHT, 7.5 µm aperture within dose factor window of 360 µC to 520 µC.

Optimization recipe for 100nm Silicon pillar etching

The control of the aspect ratio of the fabricated silicon nanostructures can be demonstrated by varying the RIE (reactive ion etching) power during the RIE process [17]. In our process of RIE, for reactive ion etching of silicon for making nano pillars with AMAT etch tool with RF Power of 800 W & Biased Power of 80 W, there were two

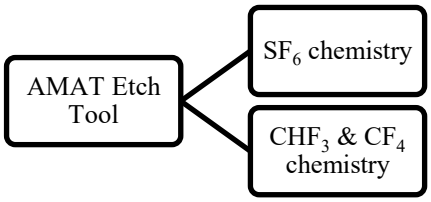


Fig. 4. AMAT etch tool methods

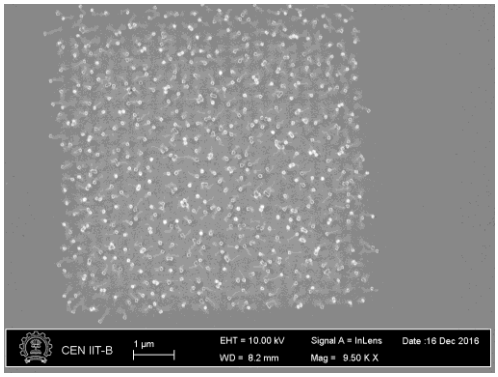
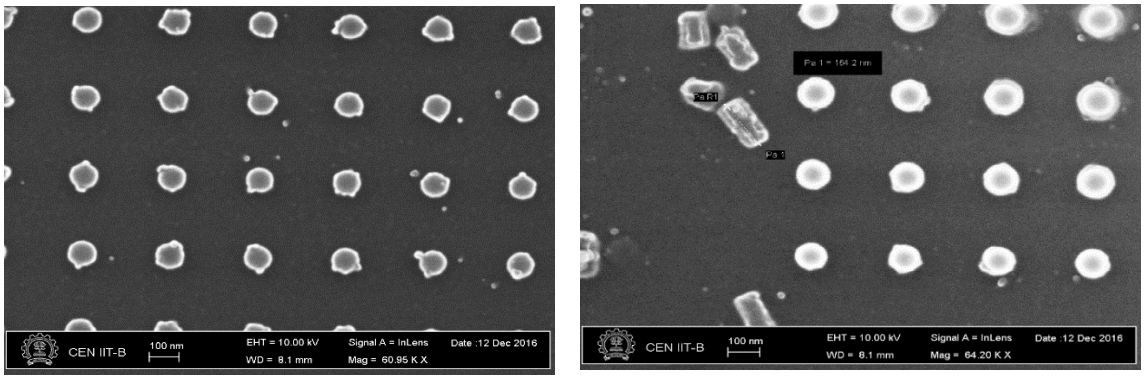


Fig. 5. AMAT etched for 30 sec using SF_6 (Si + HSQ)



a) Dose-190 **b) Dose-185**

Fig. 6. AMAT etched for 10 sec using CHF_3 and CF_4 chemistry (Si + HSQ)

chemistries available for Silicon Etching as shown in Fig. 4 below.

AMAT etching using SF_6 Chemistry

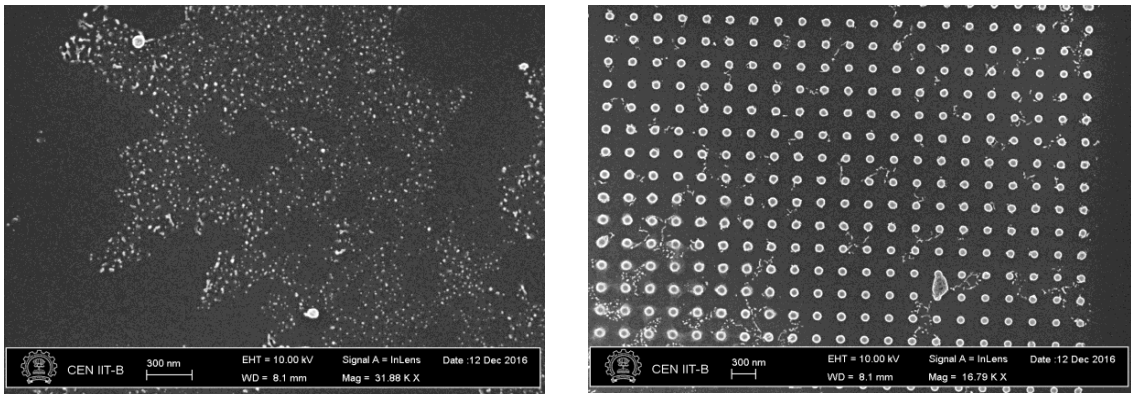
We tried SF_6 chemistry on AMAT etching tool using recipe keeping RF Power at 800 W, Biased Power at 80 W Pressure of 15mTorr, Gas used SF_6 of 110sccm. Etch rate calculated earlier to15nm/sec with Time of 30 sec. As seen from fig. 5, this SF_6 chemistry was too strong and powerful that patterned itself got white washed. But at the same time, we tried the CHF_3 and CF_4 chemistry and the results were somewhat encouraging. This is elaborated henceforth.

AMAT etching using CHF_3 and CF_4 Chemistry

The CHF_3 and CF_4 chemistry was tried on AMAT etching tool using following recipe. Taking lead from earlier AMAT experiment with SF_6 chemistry, this time, the power was lowered to 500 W so as to protect the written pattern from getting damaged. The experiment was carried out with the recipe of keeping RF Power at 500-Watt, Biased Power of 50-Watt, Pressure of 15mTorr, Gas: CHF_3 of 10sccm, CF_4 of 100 sccm and Time set was for 20 sec. Fig. 6 & 7 shows the results of AMAT etched using CHF_3 and CF_4 chemistry (Si + HSQ) for 10 secs and 20 secs respectively.

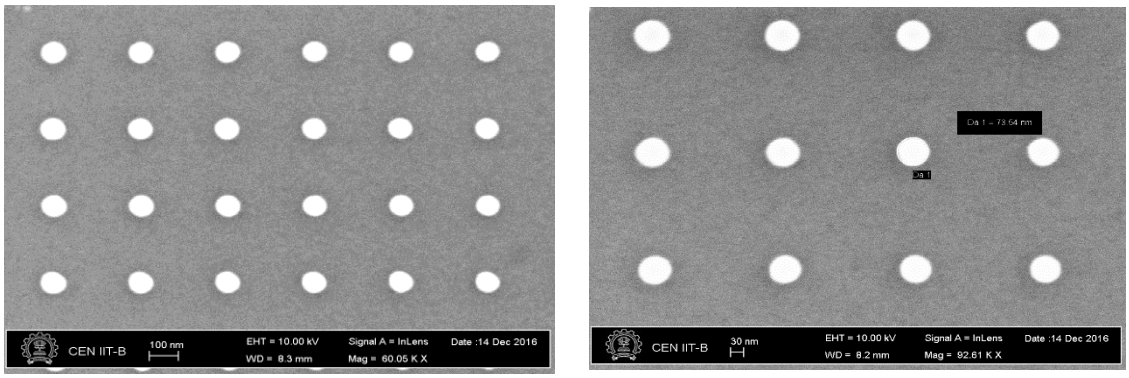
The results obtained were found good compared to AMAT SF_6 chemistry etching experiments. Some fallen pillar of 163 nm height was spotted in SEM. The surface was also less roughened. Atomic force microscopy (AFM) results confirmed the surface roughness.

The results obtained with AMAT CHF_3 and CH_4 chemistry showed good signs that it can be more optimized for getting better results. So, the next strategy was to reduce the RF power as low as



a) Surface roughness **b) Dose – 430 µC/cm²**

Fig. 7. AMAT etched for 20 sec using CHF_3 and CF_4 chemistry (Si + HSQ)

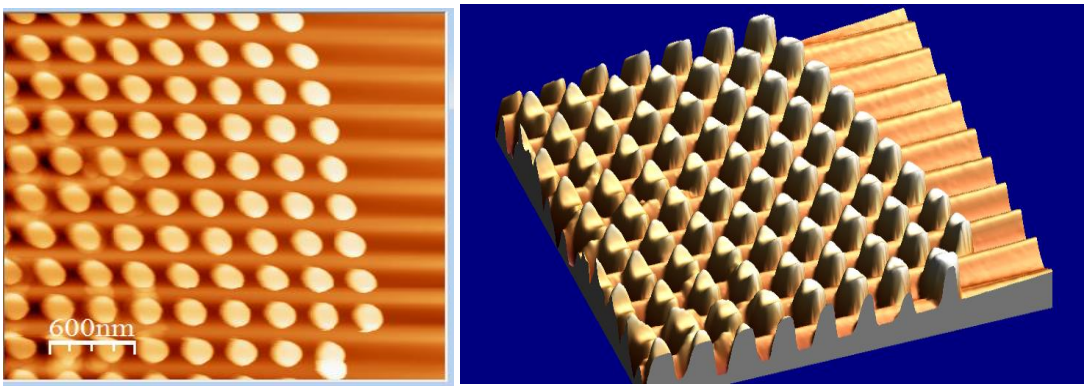


a) Dose – 390 µC/cm² **b) Dose – 400 µC/cm²**

Fig. 8. AMAT etched for 60 sec using CHF_3 and CF_4 chemistry (Si + HSQ)

possible to get the controlled and faithful etching. Thus, next experiment was carried out with the following recipe.

RF Power of 400-Watt, Biased Power of 80-Watt, Pressure at 15mTorr, Gas used was CHF_3 for 10sccm, CF_4 for 100sccm, Total Time 30 secs for sample 1 & 60 secs for sample 2. These were the best results we obtained for etching. Fig. 8 shows



(a) 2 D AFM Image **(b) 3 D AFM Image**

Fig. 9. AFM surface image for Plasma etched for 2 min using CHF_3 and O_2 gases (Si_xN_y + HSQ)

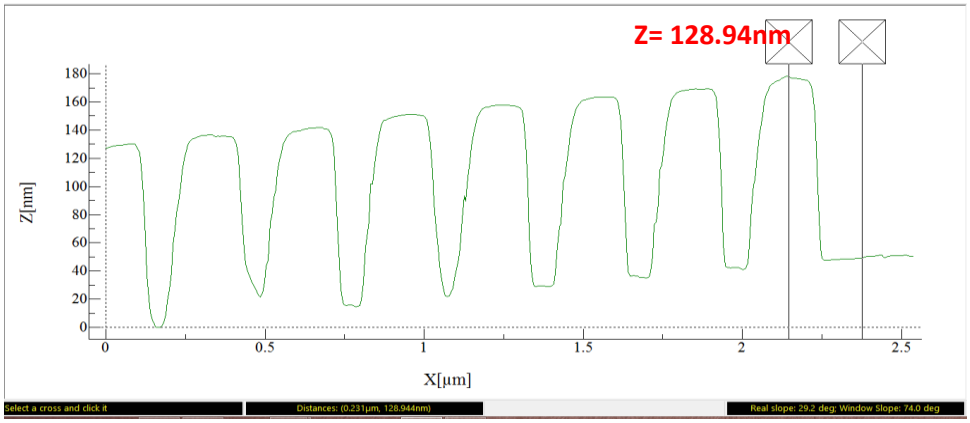
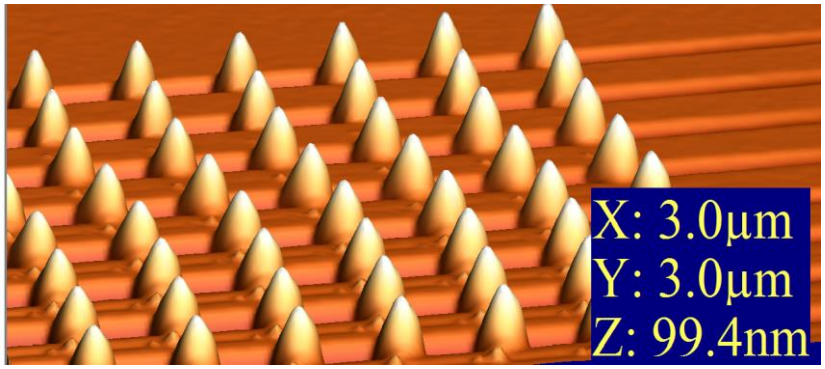


Fig. 10. AFM profile measurement for Plasma etched for 2 min using CHF_3 and O_2 gases (Si_xN_y + HSQ)



3-D AFM image with amplitude information

Fig. 11. AFM surface image for AMAT etched for 60 sec using CHF_3 and CF_4 chemistry (Si + HSQ)

Table 1. AMAT etching experiment

Sr. no	AMAT recipe	Etching time (seconds)	Height of pillar (nm)
1	RF Power - 400 W, Biased Power- 80 W Pressure - 15mTorr Gas: CHF_3 – 10sccm CF_4 – 100sccm	30	170
2		60	78

Table 2. AMAT etching experiment for different samples

Sr. no	AMAT recipe	Samples	Etching time (seconds)	Height of pillar (nm)
1	RF Power - 400 W, Biased Power- 80 W Pressure - 15mTorr Gas: CHF_3 – 10sccm CF_4 – 100sccm	S_1	20	100
2		S_2	25	
3		S_3	30	
4		S_4	35	
5		S_5	40	
6		S_6	45	
7		S_7	50	
8		S_8	55	

the result of AMAT etched for 60 sec using CHF_3 and CF_4 chemistry (Si + HSQ).

Now the task was to measure the height of silicon pillar obtained and thereby, optimize the etching time. Fig. 9 shows the AFM surface image for Plasma etched for 2 min using CHF_3 and O_2 gases (Si_xN_y + HSQ) whereas AFM profile measurement for Plasma etched for 2 min using CHF_3 and O_2 gases (Si_xN_y + HSQ) is given in Fig. 10. AFM surface image for AMAT etched for 60 sec using CHF_3 and CF_4 chemistry (Si + HSQ) is shown in Fig. 11 specifying 3-D AFM image with amplitude information.

RESULTS AND DISCUSSION

The Table 1 below summarizes the result obtained from AMAT etching experiment. After Studying the results obtained, it came to notice that for 30 sec etching time, if the nano pillar height obtained is 170nm, then for 60 sec etching time, the nano pillar height obtained was 78 nm. This observation made it clear that HSQ's masking effect is vanishing in between some range of 30 to 60 sec time. And thereafter, pillar etching is again started and so height of nano pillar is diminished at 60 sec time. Gold was vaporized on a flexible material, using electronic beam lithography to create the flexible electrode. Since Gold acts as flexible electrode [18]. Substrates made of gold-coated silicon dimer-nanopillar arrays have high sensitivity and reproducibility [19].

Thus, now task is of optimizing the etching

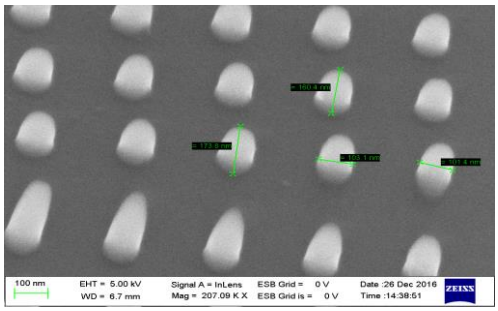
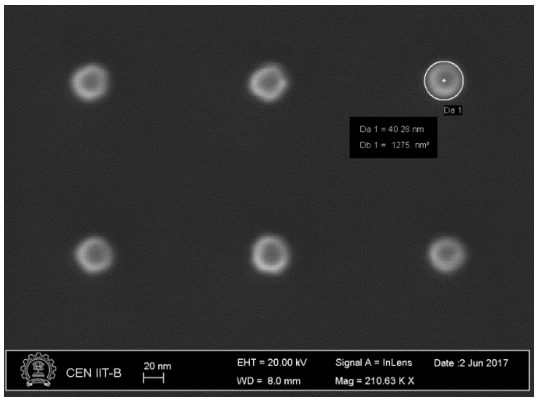
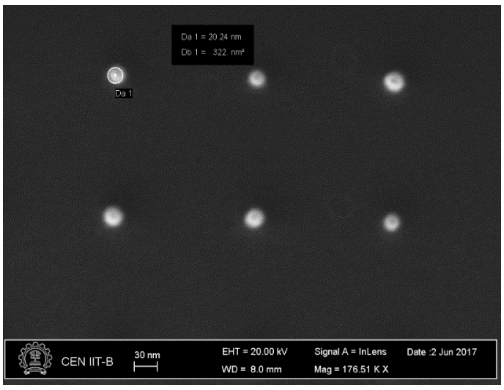


Fig. 12. FESEM image taken at tilt of 45˚for AMAT etched using CHF_3 and CF_4 chemistry (Si + HSQ)





a) SEM image after thermal curing of HSQ **b) SEM image after etching cured sample (Si + HSQ)**

Fig. 13. SEM image after thermal curing of HSQ & after etching cured sample (Si + HSQ)

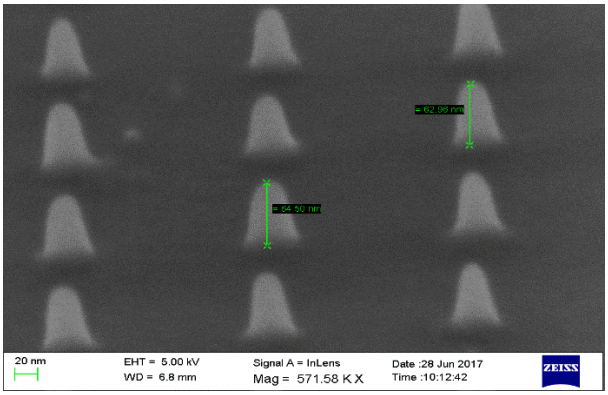


Fig. 14. FESEM image taken at tilt of 60˚for cured sample using CHF_3 and CF_4 chemistry (Si + HSQ)

time and improving the etching profile for getting the highest possible silicon pillar with HSQ resist of thickness 100nm as mask. So, eight Si+ HSQ samples were EBL patterned and etched with varying times as summarized below in Table 2.

The Field Emission Scanning Electron Microscopy (FESEM) results:

Following Fig. 12 shows the FESEM image taken at tilt of 45˚ for AMAT etched using CHF_3 and CF_4 chemistry (Si + HSQ) with 30 sec etch time. The Field emission scanning electron microscopy (FESEM) images needed more tilt like 60˚ angle for getting better overview of the height of pillars. So, the FESEM imaging also needs to be done with

more proficiency to have overall good results.

In the pursuit to increase aspect ratio of Si pillars, two more experiments were carried out like hardening of HSQ by thermal curing in oven by baking at 300C and the other one like Ultra Violet (UV) blanket exposure at higher doses like 1000mJ/cm^2. But the effect observed was patterns were shrinking. Nanoimprint lithography (NIL) involves complex post processing design steps to obtained deep nanostructures [20]. As such fig. 13 manifests the reduction of diameter from 60 nm just after EBL to 40 nm after baking in oven and further to 20nm after etching showing SEM image after thermal curing of HSQ & after etching cured sample (Si + HSQ).

The tilt FESEM image for the above thermally cured and etched Si sample is shown in Fig. 14.

CONCLUSION

After so many optimization experiments carried out, it can be inferred that AMAT etching using CHF_3 and CF_4 chemistry worked out for better pattern transfer to form Silicon nano pillar. After experimenting with different samples with different resist spinning & etching time, the results obtained was noted such that if the nano pillar height obtained is 170 nm for 30 seconds etching time; then for 60 seconds etching time, the height of the nano pillar obtained is 78 nm. This observation made it clear that the masking effect of HSQ vanishes in a range of 30 to 60 seconds. And then, pillar etching is started again, so at 60 seconds, the height of the nano pillar is reduced. We successfully implemented the nanopillar of 170 nm with AMAT recipe. In Future Scope since for GAA TFET, the pillar height required for fabrication is 250-300 nm. So, some more optimization with resist spinning and etching chemistry will be required to do further. The proposed HSQ optimization method for implementation of Nanopillar found innovative and simple due to better convenience of pattern transfer and selectivity from resist to various materials.

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CONFLICT OF INTEREST

The authors declare that there is no conflict of interests regarding the publication of this manuscript.

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