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RESEARCH PAPER

Implementing Expanded Source Doping to Improve Performance of a Nano-scale Fully Depleted Silicon on Insulator Transistor

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ABSTRACT

In this paper, we proposed a short channel Silicon on Insulator Metal-oxide Semiconductor-Field-Effect-Transistor (SOI-MOSFET), in which a thin layer of n^+-type doping has been expanded from top of its entire source region into the channel and also a proportionally heavily p-type retrograde doping has been implanted in its channel, close to the source region. Due to source doping expansion in the channel, we call this structure as Source Expanded Doping Silicon on Insulator (SED-SOI) structure. This expanded n^+ doping increases the carrier concentration in the source, which can be injected into the channel. Moreover, it increases the amount of carriers, which can be controlled more effectively by the gate electrode. These two advantages enhance both ON state current and transconductance in the device more than 1.9 mA and 5 mS, respectively. Engineered p-type retrograde doping profile causes impurity scattering and this reduces electron mobility in the depth of the device channel, which in turn OFF current decreases down to 0.2 nA. An immense comparison among our proposed device and a conventional structure (C-SOI) shows that it has better performance in terms of I_{on}/I_{off} ratio (>9.5×10^5), subthreshold swing (75 mV/dec), leakage current, breakdown voltage, hot carrier injection and DIBL. Our analysis demonstrate that SED-SOI transistor can be an excellent candidate for both low power and high performance applications.

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INTRODUCTION

Presently, the requirements in low-voltage, very-large-scale integration (VLSI) circuit designs using deep-submicron SOI CMOS technology have proceeded dramatically [1-4]. However, due to the fact that SOI devices are surrounded by oxide insulator from top and down, self-heating effect (SHE) has always been a challenging problem in this technology [5-8]. To overcome this problem, researchers in their recent works proposed new interesting structures [9-11]. The origin of this phenomenon is presence of a buried oxide layer below the active silicon region. As silicon dioxide (SiO_2) heat conductivity is very low, the generated heat along the active layer accumulates there and the lattice temperature increases. This can cause mobility and reliability degradation in these devices [12, 13].

On the other hand, as transistor dimensions are shrinking, lattice temperature, short channel effects (SCE) and leakage current problems become more serious in SOI structures [4, 14-19]. The prior problem is because of exceeding device density and power dissipation in the unit area of integrated circuits [20, 21]. Recently, several good SOI-MOSFET structures have been reported in the literature to improve aforementioned problems

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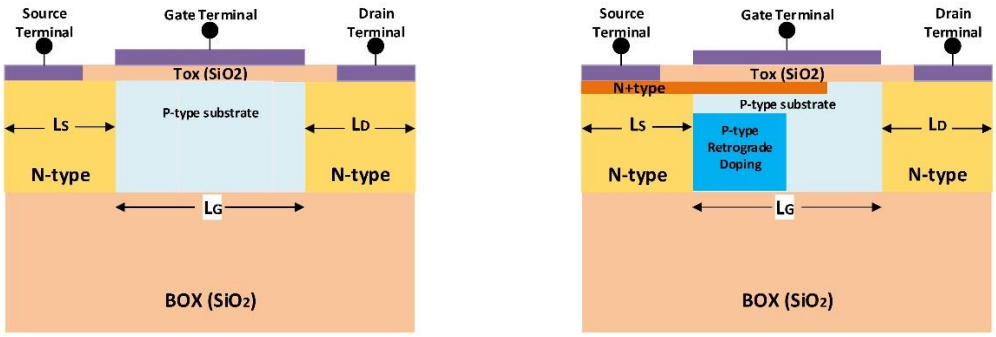


Fig. 1. Cross section view of: (a) C-SOI and (b) SED-SOI structures.

[5, 6, 22-24]. In most of them, either fabrication process steps more than ever have increased or new materials other than silicon or silicon dioxide are utilized. Though it is necessary to introduce new material and technology for future scaling, but it is clear that scaling with new materials and technologies have a huge cost in R&D process and needs new equipment and tools for mass production [21]. Although, tunnel field effect transistors (TFETs) become one of the serious candidates for more Moore, as its structure is very close to MOSFET and have very low leakage current, but these devices have the problem of ambipolar conduction at negative gate voltages and low drive current, which do not satisfy ITRS requirements [2, 3, 25, 26].

In this work, we have proposed a new transistor in SOI technology in which it demonstrates lower lattice temperature and better reliability against SCEs. In the proposed structure, p-type retrograde dopants are implanted in the depth of channel close to the source region and a thin layer of n-type doping is also expanded from top of source region until two-third of the channel. It is worth noting that the proposed structure is asymmetric and needs precise doping implantation process which this may increase the fabrication steps and cost, but our simulation results show doping engineering techniques can improve SHE and SCEs in the proposed device in comparison to C-SOI counterpart.

The rest of this paper is organized as follows. In section 2, the new structure is introduced. Simulation results are presented in section 3. Section 4, considers SED-SOI design and finally, the paper is concluded in section 5.

SED-SOI DEVICE DESIGN

Fig.1 (a-b) shows the schematic view of C-SOI and SED-SOI respectively. The aim of our proposed design is to improve I_{on}/I_{off} ratio, SCEs and device temperature, while keeping the fabrication process possible or compatible with fabrication equipments. For that, we optimized the position, length and the doping value of the extended $n^+$and retrograde dopants in the source and channel to achieve the above-mentioned goals. All geometrical and process parameters related to both structures under study are presented in Table 1.

Fig. 2 shows the fabrication flow of the SED-SOI structure. The process starts with a P-type silicon substrate at stage 1. Then, the oxygen ion implantation is done to form a buried oxide at stage 2. Stage 3 includes the Boron ion implantation for creation of the P-type retrograde doping underneath the channel. At stage 4, the phosphorus ion implantation is performed to constitute Source and Drain regions. Then, the phosphorus ion implantation with lower energy is performed at stage 5 to form Source expanded region on the surface of silicon film. Afterward, top oxide deposition is done at stage 6. After oxide etching on top of the source and drain regions (stage 7), common metallization process is done at stage 8 according to conventional SOI transistor [8].

To simulate and examine different characteristics of the proposed SOI device, 2-D ATLAS device simulator was used. In order to have reliable results, we used Fermi Dirac distribution function and non-isothermal energy balanced models to consider the effect of carrier

Table 1. Parameters for SED-SOI and C-SOI structures.

Parameter	Values	
	SED-SOI	C-SOI
Top oxide thickness (Tox)	1 nm	1 nm
Silicon channel thickness	10 nm	10 nm
Buried oxide thickness (BOX)	40 nm	40 nm
Extended N^+ doping thickness	1 nm	-
Gate Length (L_G)	15 nm	15 nm
Source/Drain Extension Length (L_S , L_D)	10 nm	10 nm
Source/Drain Electrode Length	7 nm	7 nm
Extended N^+ doping length in the channel	10nm	-
Gate Workfunction	4.6 eV	4.6 eV
Channel doping (p-type)	1e12 cm^{-3}	1e12 cm^{-3}
Source/Drain doping (n-type)	6e18 cm^{-3}	6e18 cm^{-3}
N^+ doping on top of source	6.6e19 cm^{-3}	-
Extended N^+ doping in the channel	6e19 cm^{-3}	-
retrograde doping	5e19 cm^{-3}	-
retrograde doping Width	4 nm	-
retrograde doping Height in the channel	7 nm	-

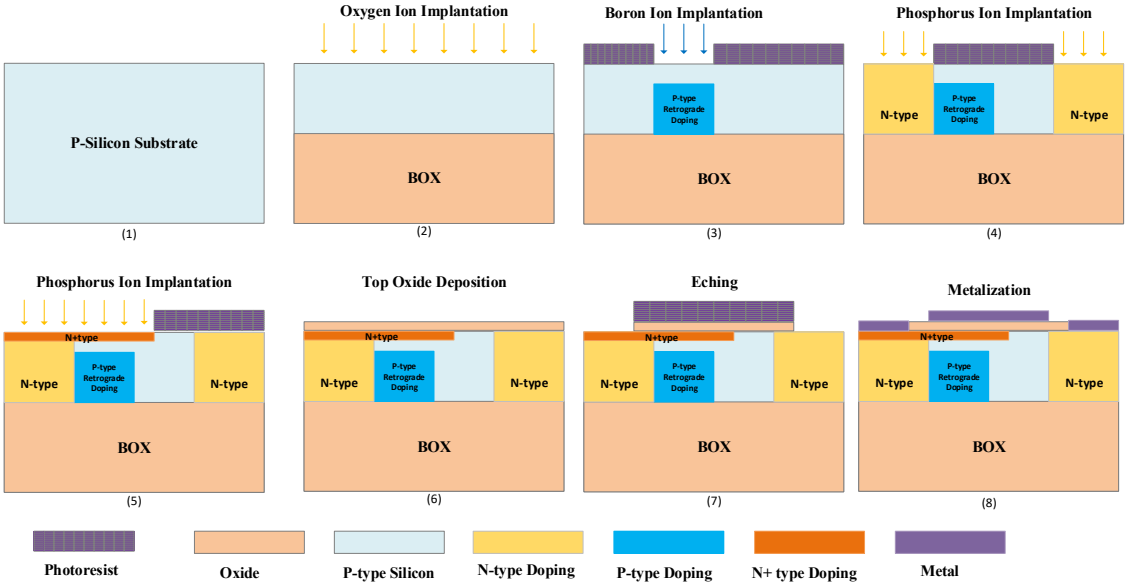


Fig. 2. The fabrication flow of SED-SOI structure.

temperature on mobility. We used SRH and Auger models to consider recombination in the device based on Shockley-Read-Hall and Auger physics [20]. FLDMOB and CONMOB models were added to consider field and concentration dependent mobility. HEI and HHI were utilized to take hot electron and hole injection effects in gate and drain contacts into account. HCTE.EL and LAT.TEMP models were also included to consider electron temperature in transport model and global device temperature. BGN model utilized to correctly account for the doping dependence of the band gap and IMAPC SELB flag enabled to model the impact ionization in simulations [27].

RESULTS AND DISCUSSION

This section includes the performance analysis and comparative study of devices shown in Fig. 1. For this, we first discuss about transfer characteristic curve (I_D-V_{GS}) which reveals many properties of a device. Fig.3 which depicts the transfer characteristic of two MOSFETs at

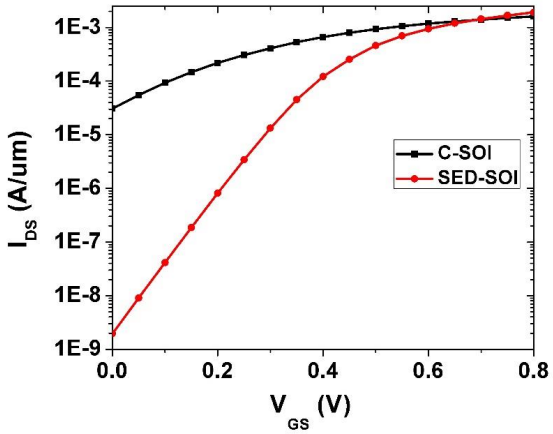


Fig. 3. Transfer characteristics (I_D-V_{GS}) for C-SOI and SED-SOI at V_{DS}=0.6V.

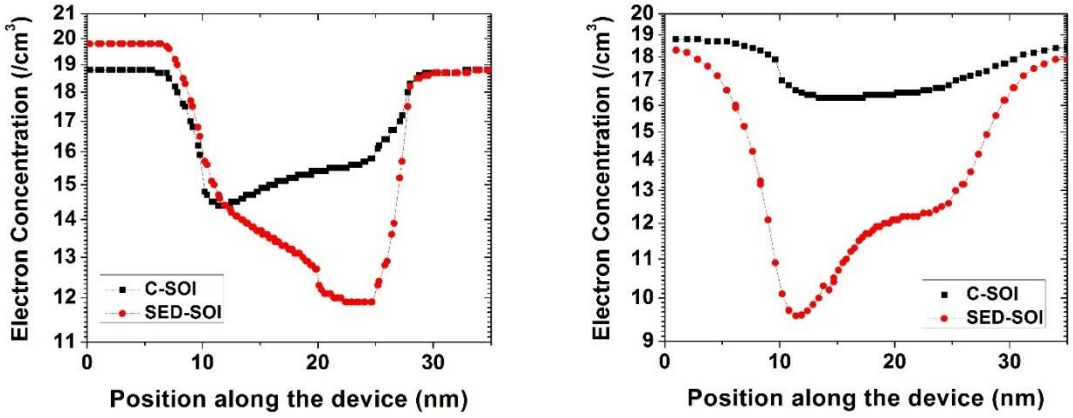


Fig. 4. Electron concentration, along (a): top of the device channel thickness and (b): middle of the device channel thickness at bias V_{DS}= 0.6 V and V_{GS}=0 V.

V_{DS}=0.6V, confirms the excellence of SED-SOI with respect to its C-SOI counterpart in terms of higher ON current, lower leakage current and better subthreshold swing (SS). The lower leakage current in SED-SOI origins from the retrograde doping profile in the depth of the channel. Fig. 4 which depicts electron concentration along the top and middle of the channel thickness at bias V_{DS}= 0.6 V and V_{GS}=0 V, which corresponds to OFF condition, confirms this claim. Indeed, retrograde doping scatters electrons passing from depth of the channel and limits their effective passage mostly from the top region of the channel. In fact, the effective channel thickness is virtually reduced and gate control over the channel is improved. When a positive gate voltage is applied, since there are electrons with higher concentration on top of the channel due to the presence of expanded n^+ doping region, ON current in our proposed device increases rapidly, and at V_{GS} > 0.7 V the current becomes more than C-SOI drive current as shown in Fig. 3. The energy band diagram of the proposed device is shown in Fig. 5 (a). This figure can help us to find the physical reason behind suppression of short channel effect in the proposed structure. Fig. 5 (a) shows both conduction and valence bands of the proposed device stays on top of the corresponding bands of the conventional device, which means SED-SOI is more persistence against drain induced barrier lowering (DIBL) which is an important short channel effect. In fact, the potential barrier between source and channel is

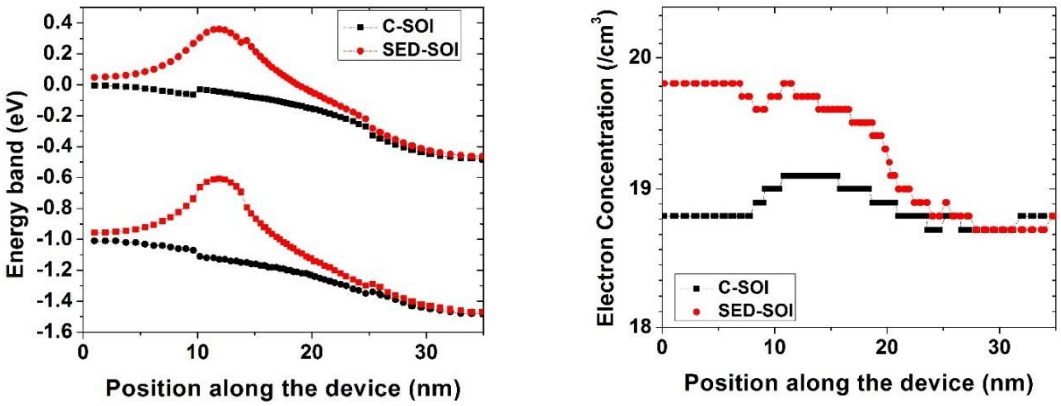


Fig. 5. (a): Energy band diagram along the device, (b): electron concentration along top of the device at bias V_{DS}= 0.6 V and V_{GS}=0.8 V.

less affected by the drain bias in SED-SOI and thus the DIBL is more suppressed due to retrograde doping profile close to the source. The expanded n^+ doping in the channel profile causes carriers to pass from the top region of the channel. This is in agreement with the results we obtained from the simulation of electron concentration along the device channel and is illustrated in Fig. 5(b). Moreover, the channel length is virtually reduced which in turn leads to further increase of ON current in comparison with the conventional device. In this situation gate electrode has better electrostatic control over a desired region of the channel where more carriers pass from it. This helps lowering SS in SED-SOI. According to SS concept, lower SS provides faster transition of the device between ON and OFF states. The values of SS for SED-SOI and C-SOI are 75 and 200 mV/dec, respectively.

In Analogue devices, the amount of amplification is a figure of merit. Intrinsic gain is defined by the following relation [28]:

$$Gain = \frac{g_m}{g_d} \quad (1)$$

where g_m and g_d are transconductance and output conductance of the device respectively [21,22], given by:

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{V_{DS}=const} \quad (2)$$

$$g_d = \left.\frac{dI_D}{dV_{DS}}\right|_{V_{GS}=const} \quad (3)$$

Higher value for g_m in a device means that the gate has better control over drain current variation [29]. Therefore, it is desired that a device exhibits high value of transconductance. According to the Fig .6, transconductance curve of SED-SOI is close to ideal form. This is due to the fact that at subthreshold voltages where the device is in OFF state, there will not be enough current for amplification and g_m is close to zero. However, by sweeping the gate voltage above the threshold voltage when MOSFET becomes ON, g_m suddenly increases and it gets ready to increase the current controllability by the gate electrode as well as more amplification. Transconductance behavior in C-SOI is not satisfactory, because it is high in subthreshold voltages and low at the "above threshold" region. Fig. 7 illustrates that SED-SOI has lower output conductance (g_d) in most of gate voltages compared with C-SOI. As an important result and based on Eq. (1), SED-SOI exhibits much more intrinsic gain with respect to C-SOI MOSFET. Device temperature in SOI MOSFETs is a serious problem, as device is surrounded by insulator and there is not easy path for the produced heat to pass from. Fig .8 presents global device temperature of two MOSFETs. It is clear that SED-SOI has much lower temperature in comparison to its counterpart at all gate voltages.

Our simulation results shows even at equal drain current for two devices, the temperature of our proposed device is about 10°K cooler than C-SOI. The reason for lower impact ionization rate of SED-SOI in comparison with C-SOI is investigated based on Fig .9. In fact, when electrons pass from the channel in C-SOI MOSFET, they collide with atoms close to the drain region, where they obtain

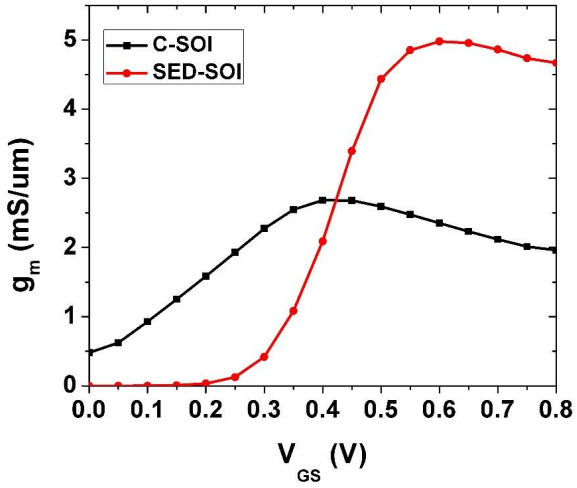


Fig. 6. Transconductance in C-SOI and SED-SOI at V_{DS}=0.6 V.

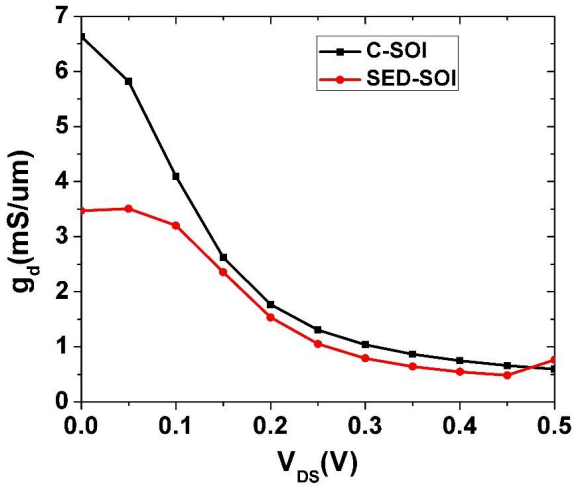


Fig. 7. Conductance in C-SOI and SED-SOI at V_{GS}=0.6 V.

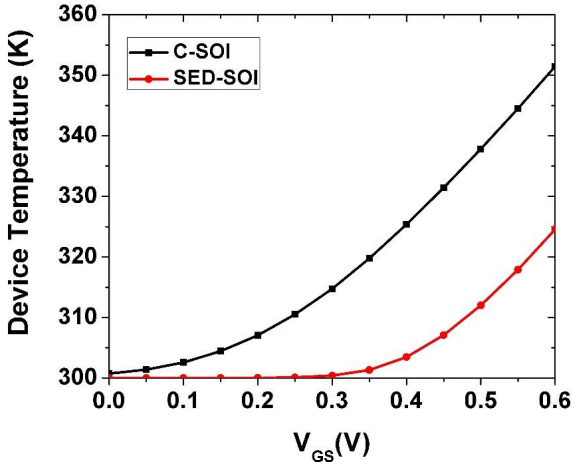
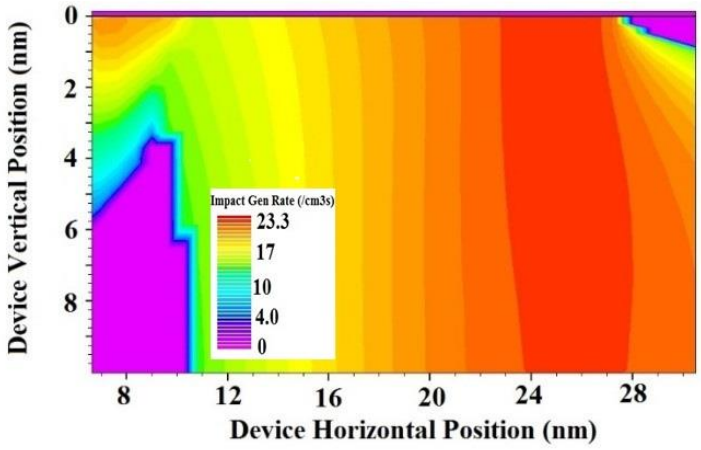
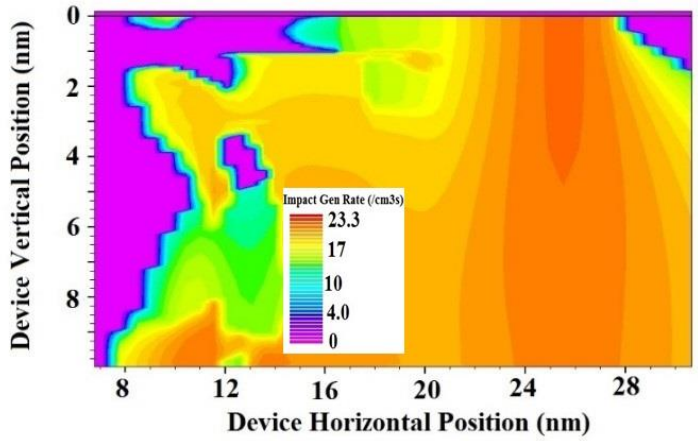


Fig. 8. Global device temperature in C-SOI and SED-SOI MOSFETs at V_{DS}=0.5V.



(a)



(b)

Fig. 9. Impact generation rate in: (a) C-SOI and (b) SED-SOI, at V_{DS}=0.5 V and V_{GS}=0.6 V.

highest kinetic energy and cause the Si-Si bonds to break down. These collisions produce hot electrons and holes, which increase the device temperature. These hot carriers may have enough energy to pass from the gate oxide insulator or barrier and then enter the gate electrode and cause gate leakage current. Fig. 10 and Fig. 11 show that both hot electron and hot hole currents in the gate of SED-SOI is lower in comparison to C-SOI MOSFET, respectively. The presence of retrograde doping in SED-SOI reduces electron acceleration along the channel, due to immobile acceptor (impurity) scattering in the retrograde doping region; and this causes lower impact ionization in the proposed device. These results emphasize our proposed device reliability against other short channel effects: hot carrier degradation and impact ionization. It should be noted that gate hot hole current has been stated in absolute value, because some of hot holes after existence are propelled to the gate positive voltage, affected by drain higher potential.

In the aerospace applications, the MOSFETs employed in electronic equipments are more exposed to energetic space rays. These rays can threaten MOSFETs reliability in their persistence against higher unexpected voltages. Breakdown voltage is a good measure to consider this issue. This parameter has seriously considered in the literature [30-33]. Also it is mostly mentioned in

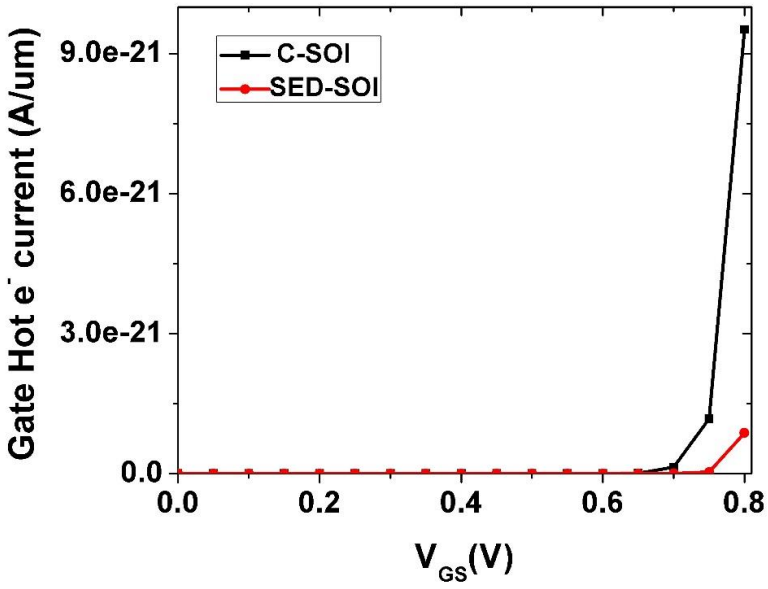


Fig. 10. Gate hot electron current for C-SOI and SED-SOI at V_{DS}=0.6 V.

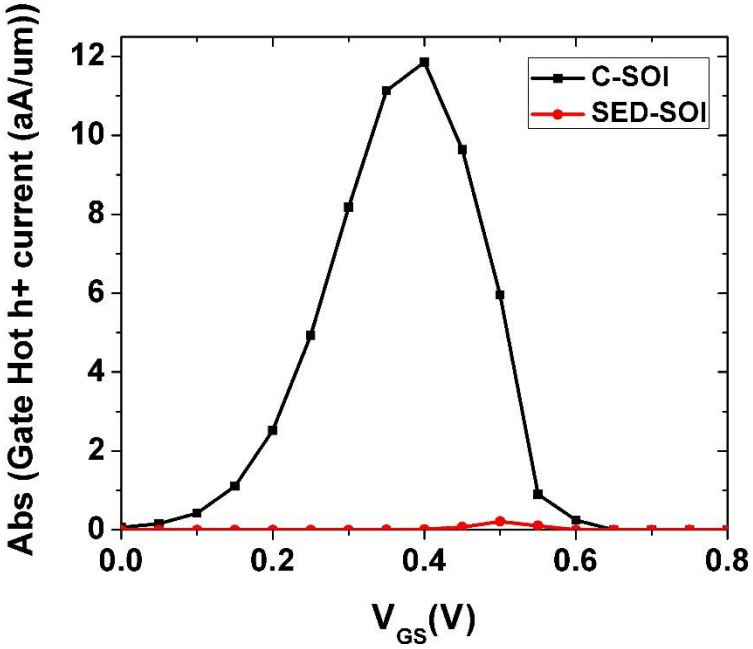


Fig. 11. Absolute value of gate hot hole current for C-SOI and SED-SOI at V_{DS}=0.6 V.

high voltage and smart-power applications, where they also offer the advantage of compatibility with VLSI processes. Fig. 12 depicts breakdown voltage of two MOSFETs and confirms SED-SOI has more than 10 times higher breakdown voltage and reliability with respect to its counterpart. This higher breakdown voltage in our proposed device origins from lower collisions, less hot carriers and lower device temperature as mentioned previously.

Drain Induced Barrier Lowering (DIBL) is another SCE, which considers the impact of drain

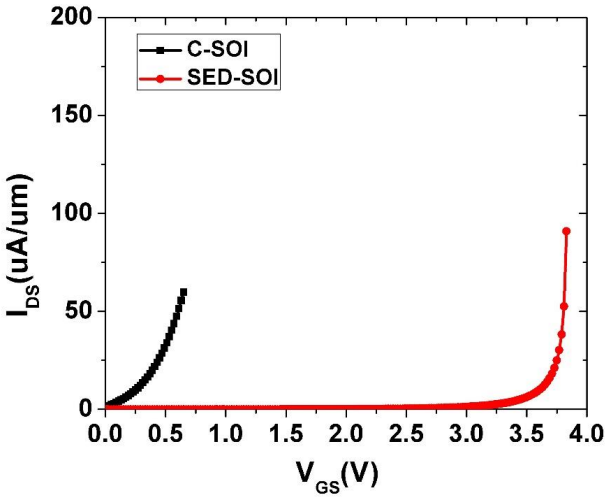


Fig. 12. Breakdown voltages of SED-SOI and C-SOI at V_{GS}=0 V.

Table 2. DIBL value of two devices.

	V_{g1} (V)	V_{g2} (V)	DIBL (mV/V)
C-SOI	0.213	0.0677	364
SED-SOI	0.404	0.358	116

Table 3. Comparison of I_{ON}/I_{OFF} ratio, subthreshold swing, DIBL and maximum lattice temperature of SED-SOI with other published works.

Parameter	This work	[35]	[11]	[37]
I_{ON}/I_{OFF}	9.5×10^5	53×10^4	-	1×10^2
SS (mV/dec)	75	74	-	550
DIBL (mV/V)	116	215	-	-
Max lattice temperature(K)	325	-	470	300

bias on the lowering of the channel conduction band. This phenomenon is a problem in the short channel devices and should be as low as possible because it leads to leakage current and threshold voltage variation because of changing the drain bias. In order to consider DIBL effect in a device, we use the following relation:

$$DIBL = \frac{V_{g1} - V_{g2}}{V_{DS2} - V_{DS1}} \quad (4)$$

where V_{g1} and V_{g2} are gate voltages corresponding to the drain current of I_{DS}=1E-4 A at V_{DS1}=0.3 V and V_{DS2}=0.7 V respectively. It should be noted that the mentioned drain current value is quite optional and we chose it according to device curves. From Table 2, it is clear that DIBL effect is less for the proposed device and SED-SOI is more persistence against this SCE. The main reason of DIBL improvement in SED-SOI is using p-type doped region close to the source, which acts like an obstacle against drain voltage to affect source side anymore. As we mentioned earlier, Fig. 5 (a) confirms DIBL improvement in SED-SOI visually.

Finally, Table 3 compares some important figure of merits in this work (SED-SOI) with other published works in the field of SOI MOSFET in terms of I_{ON}/I_{OFF} ratio, subthreshold slope, DIBL effect and maximum lattice temperature which are presented in this table. It is obtained that our proposed device shows in total higher I_{ON}/I_{OFF} current ratio and comparable SS, DIBL and lattice temperature amounts compared with references [11,35, 37].

SED-SOI DESIGN CONSIDERATIONS

One of the main reasons for proposing the new structure was I_{ON}/I_{OFF} ratio improvement. For that, we start with I_{OFF} reduction. An idea to

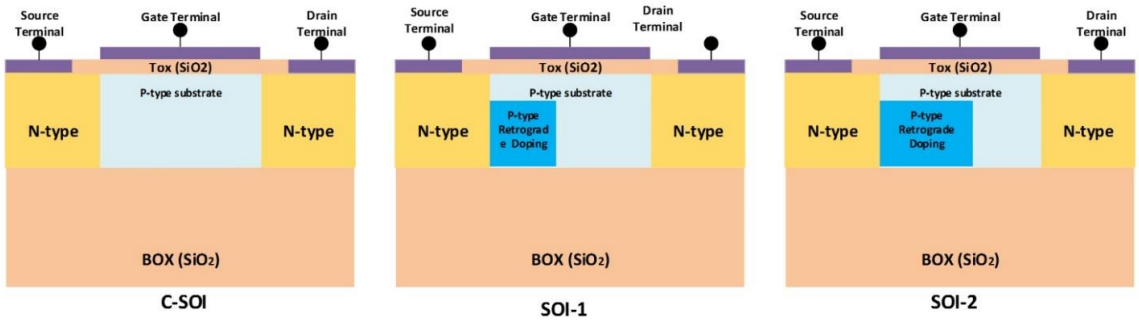


Fig. 13. Cross section view of: C-SOI, SOI-1 and SOI-2 structures.

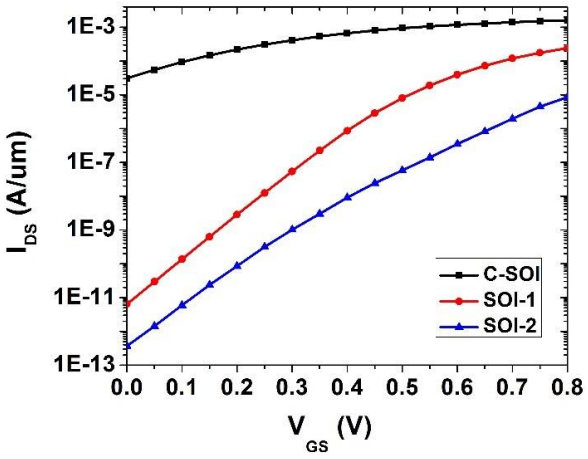


Fig. 14. Transfer characteristics (I_D-V_{GS}) for C-SOI, SOI-1 and SOI-2, at V_{DS}=0.6V.

decrease leakage current, is implementing p-type retrograde doping at the depth of the channel. This idea has two physical reasons and benefits. First, it helps short channel effect to reduce; and second, acceptor dopants can cause electrons to be scattered when passing from the depth of the channel where the gate control is weaker. In fact, we want to decrease effective channel thickness for electrons, virtually. So, we set an experiment to find the optimum dimensions for p-type retrograde doping according to Fig. 13, where C-SOI electrical characteristics is compared with two other devices, SOI-1 and SOI-2. We set retrograde doping concentrations amounts according to p_1=p_2= 5e19 cm^{-3} and sweep the retrograde doping width to W_1=4 nm and W_2=8 nm for SOI-1 and SOI-2 MOSFETS, respectively and other device parameters are kept fixed according to Table 1. Fig. 14 shows transfer characteristics of three devices under study. According to this figure, as retrograde doping widens, OFF-current decreases and threshold voltage increases. In fact, when p-type retrograde doping is used in the channel, gate terminal needs more effort to deplete the channel and this increases the threshold voltage of device. So, due to impurity scattering in the depth of the channel and then threshold voltage enhancement, the drain electric field influence reduces on carriers moving from source to drain through the channel and this decreases OFF state current. Thus, we expect that the statics power consumption to be reduced in SOI-1 and SOI-2 structures. Table 4 which reports subthreshold swing and threshold voltage of three devices under study, acknowledges SOI-1 has better electrical characteristics, i.e. lower subthreshold swing and acceptable threshold voltage with respect to supply voltage of 0.6- 0.7 V. Therefore, in the following we choose SOI-1 for next step of experiments.

In the next step we are going to improve ON-current. The idea is incorporating a thin layer of n-type doping on top of the source and channel, in order to increase the number of carriers which

Table 4. Subthreshold swing (S) and threshold voltage (Vth) for three structures.

	C-SOI	SOI-1	SOI-2
SS (mV/dec)	200	75	85
Vth (V)	-0.145	0.32	0.42

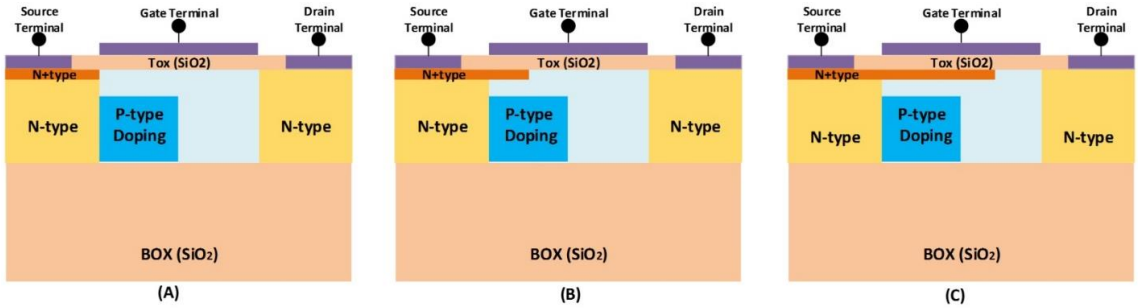


Fig. 15. Cross section view of: SOI structures with expanded doping which covers (a) 0 nm, (b) 5 nm and (c) 10 nm along the channel.

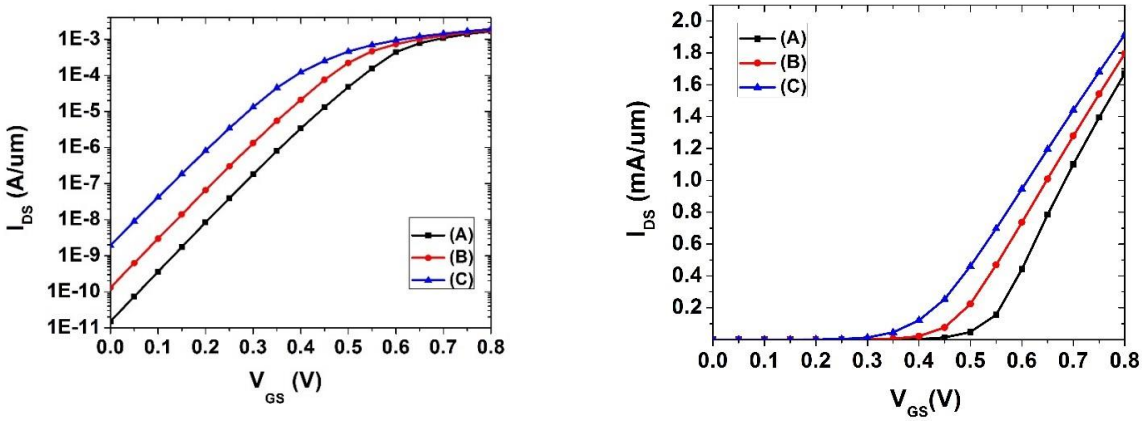


Fig. 16. (a)-logarithmic, and (b)-linear presentation of transfer characteristics (I_D-V_{GS}) for structures (A), (B) and (C), at V_{DS}=0.6V.

can effectively impress on drive current while are completely under control of gate terminal. For this, we sweep the n^+ expanded doping length along the top of source and channel in three structures under study as shown in Fig. 15. According to this figure, expanded doping covers top of source region plus 0, 5 nm, and 10 nm of the channel while other device parameters are kept fixed according to Table 1. As Fig. 16 depicts, ON current in these structures increase compared to SOI-1 device characteristics in Fig. 14 which this can enhance the device speed. Although OFF current has also increased in these cases, but they are less than 2nA and I_{ON}/I_{OFF} current ratio is more than 9.5×10^5 which is acceptable [28].

In a FD-SOI, the following relation describes drain saturation current [2]:

$$I_{Dsat} = \frac{1}{2n}\frac{W}{L}\mu_n C_{ox}[V_{GS} - V_{th}]^2 \quad (5)$$

Where n is body effect coefficient, C_{ox} is oxide capacitance, μ_n is electron mobility and W and L are channel width and length, respectively. The presence of extended source doping virtually decreases the channel length when the device is in ON state. So, according to above relation, drain saturation current increases. On the other hand, as the channel length scales, the threshold voltage will be reduced. Therefore, we expect that extended source doping also decreases V_{th} and

thus drain current will be further enhanced.

In order to examine this channel length reduction, we first estimate the body factor coefficient (*n*) based on Eq. (5) for the pristine case (the device with no extended source doping where $L=L_{eff}$=15 nm). Then we will use this body factor coefficient to estimate effective channel length of other devices. The device width is assumed to be 1 µm. The electron mobility is assumed to be 78.8 cm^2/V.sec [20]. The oxide capacitance can be calculated from the oxide thickness as given in Table 1. The resultant body factor will be 2.71. Considering $I_{Dsat,A}$=1.672 mA, $I_{Dsat,B}$=1.796 mA and $I_{Dsat,C}$=1.915 mA from the I_d-V_g transfer characteristics shown in Fig. 16(b), and extracting the threshold voltages from the constant current criteria method [12] as $V_{th,A}$=0.3 V, $V_{th,B}$=0.4 V and $V_{th,C}$=0.45 V; Eq. (5) gives $L_{eff,A}$=15 nm, $L_{eff,B}$=8.94 nm and $L_{eff,C}$=6.4 nm. This shows that an effective channel length reduction happens because of the extended source region.

We know as the channel length decreases, both drive current and leakage current increase. In fact, by this trick we could virtually decrease the channel length, and utilized its benefits mostly on the drive current. Based on Fig. 16, subthreshold swing of three devices are almost equal to SS= 75 mV/dec while the threshold voltages are shifting. Because structure (C) has higher drive current, lower threshold voltage with acceptable leakage current in VLSI, compared with structure (A) and (B), it can be also suitable for high performance applications.

CONCLUSION

Source expanded doping into the channel of a SOI-MOSFET can lead to increased ON current and lowered device temperature in the active region of the device by reducing electron collisions and increasing the mobility. Thus, self-heating effect improved in comparison with C-SOI. Moreover, combination of P-type retrograde doping in the channel and source expanded doping was proposed to reduce the leakage current, increase I_{ON}/I_{OFF} ratio, and decrease the subthreshold swing and to improve the SCE effects like DIBL and hot carrier injection. According to above-mentioned benefits, the SED-SOI MOSFET can be an appropriate candidate in realization of VLSI integrated circuits particularly in low power and high performance applications.

CONFLICT OF INTEREST

The authors declare that there are no conflicts of interest regarding the publication of this manuscript.

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