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# Effects of the Spacer Length on the High-Frequency Nanoscale Field Effect Diode performance

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**Abstract**

The performance of nanoscale Field Effect Diodes as a function of the spacer length between two gates is investigated. Our numerical results show that the $I_{on}/I_{off}$ ratio which is a significant parameter in digital application can be varied from $10^1$ to $10^4$ for S-FED as the spacer length between two gates increases whereas this ratio is approximately constant for M-FED. The high-frequency performance of FEDs is investigated and the cut-off frequency of the intrinsic transistor without parasitic capacitance is calculated. The figures of merit including intrinsic gate delay time and energy-delay product have been studied for the field effect diodes which are interesting candidates for future logic applications.

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## 1. Introduction

According to the Moore's law, miniaturization of Si devices is reaching its limits. However, ultra scaled transistors suffer from short channel effects. By employing a Field Effect Diode (FED) structure one can improve such effects [1]. The performance of digital and analog circuits can be improved by replacing conventional MOSFETs by FEDs. They have many interesting properties and applications such as electrostatic discharge (ESD) protection [2-4] and memory cells application [5, 6].

A FED is similar to a conventional MOS transistor with the exception of using two gates over the channel region and oppositely doped source and drain (see Fig. 1(a)). As the channel length shrinks to dimensions less than 100nm, the regular FED has a large off-current. To overcome this problem, modified FED (M-FED) (Fig. 1(b)) and side-contacted FED (S-FED) (Fig. 1(c)) structures have been recently proposed [7,8]. In these structures, oppositely doped regions called reservoirs are introduced to the source and drain regions [9]. FEDs have superior properties to SOI-MOSFETs, since pinch-off, which limits current in MOSFETs, does not occur in FEDs .

In this paper, the effect of the spacer length between two gates on the electrical characteristics and frequency response of M-FED and S-FED is investigated and also compared. The figures of merit including intrinsic gate delay time and energy-delay product, which represent the speed and switching energy of the device, respectively, are studied.

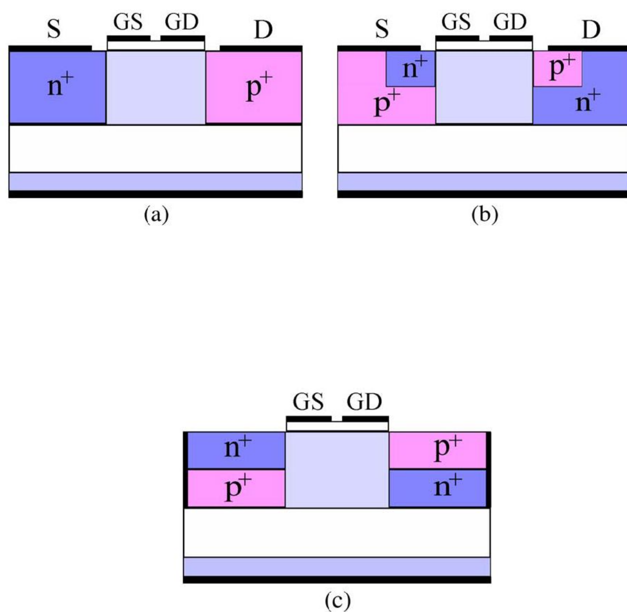


**Fig. 1.** Schematic structures of (a) regular, (b) modified and (c) side-contacted FED.

## 2. Results and discussion

The numerical device simulation results are obtained from Dessis (ISE-TCAD device simulator), which can be used to simulate nanoscale devices with an acceptable level of approximations. We have solved the Poisson and continuity equations to obtain the electrical characteristics of the FED, including I-V characteristics and carrier concentrations under each gate.

We studied FEDs with a gate length of 35nm, a body thickness of 50nm, and a gate oxide thickness of 2nm. The depths of reservoirs and source/drain regions are 50 and 25nm, respectively [10], and a device width of 1 μm. It is noted that, the channel length of the FED structure is defined as $L_{ch} = 2L_g + L_{sp}$ in which $L_g$ is the constant gate length. Therefore, as the spacer length is decreased, the channel length is decreased too.

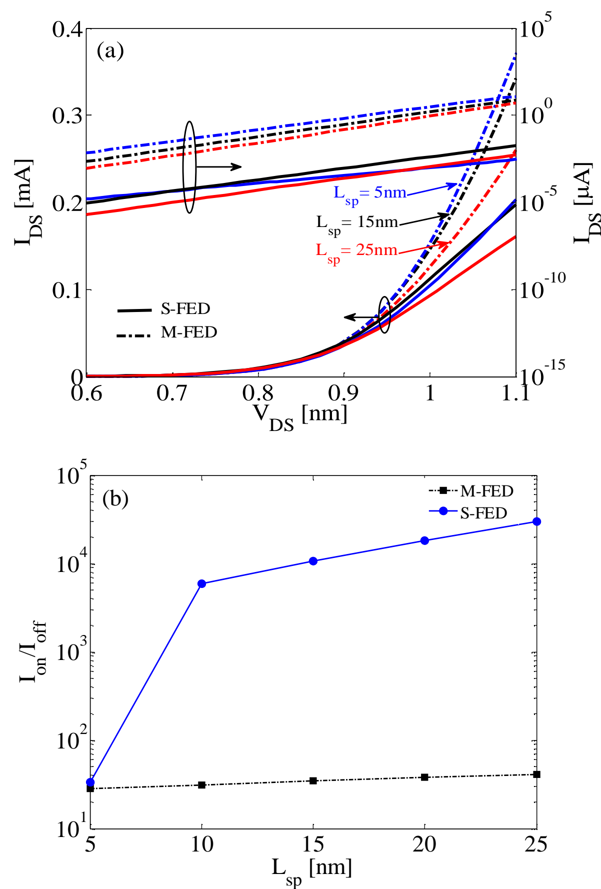


**Fig. 2.** (a) The output characteristics in the on and off state and (b) The $I_{on}/I_{off}$ ratio of the S-FED and M-FED as a function of $L_{sp}$.

The output characteristics of FED structures as a function of the spacer length ($L_{sp}$) are compared in Fig.2 (a) in the on and off state. As seen in this figure, as the gates are located far from each other, the on- and off-current will be decreased. In the

other words, as $L_{sp}$ increases, the depletion region formed under, widens, therefore, the carrier injection through this region will be decreased. As a result, the $I_{on}/I_{off}$ ratio can vary from $10^1$ to $10^4$ for S-FED, whereas this ratio is approximately constant for M-FED (see Fig.2 (b)).

The intrinsic gate delay time with respect to the $I_{on}/I_{off}$ ratio can be employed to compare devices with different geometrical and material parameters [11]. The gate delay time, which characterizes the switching response of a transistor, is an important metric for digital electronic applications. The gate delay time of a transistor is defined as the time taken to charge a constant gate capacitance $C_G$ to a voltage $V_{DD}$ at a constant current $I_{on}$:

$$\tau = \frac{C_G V_{DD}}{I_{on}} \quad (1)$$

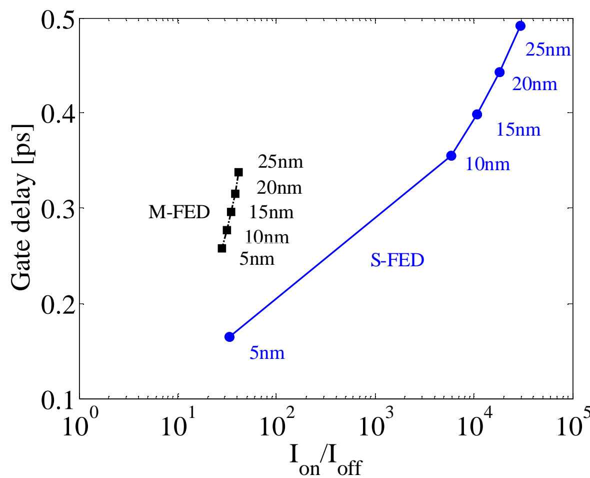


**Fig. 3.** The intrinsic gate delay time as a function of the $I_{on}/I_{off}$ ratio for various spacer lengths between gates.

Fig. 3 compares the gate delay time as a function of the $I_{on}/I_{off}$ ratio for nanoscale FEDs with different spacer length between gates. The intrinsic capacitance ($C_G$) is calculated from simulation results, by the derivation of the total charge present in the channel with respect to $V_{GS}$. The results shown in Fig. 3 demonstrate obvious advantages of FED devices. The results show that FEDs with the spacer length of 5nm have a smaller gate delay time in comparison to the other spacer lengths.

Fig.4 shows the FEDs gate delay time and EDP as a function of the $L_{sp}$. As expected, by decreasing $L_{sp}$, the gate delay time decreases. As shown in Fig.4, FEDs have the smallest delay time with $L_{sp}$=5nm. Fig.4 also illustrates that the minimum EDP belongs to S-FED whereas there is no effect on the M-FED at various $L_{sp}$ and this value is larger than that of M-FED.

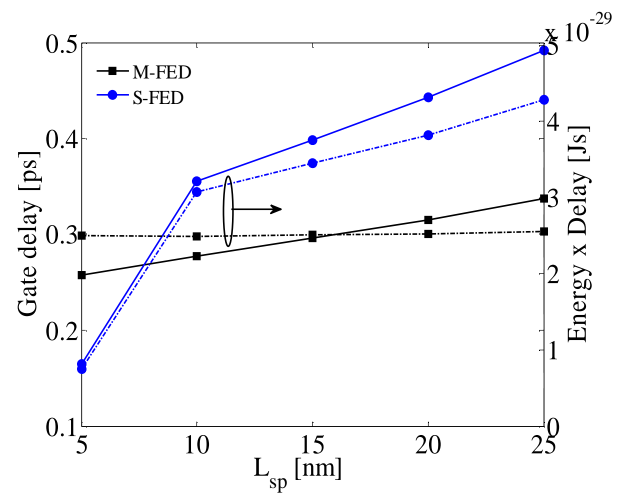


**Fig. 4.** The intrinsic gate delay time and Comparison of the energy-delay product of FEDs as a function of $L_{sp}$.

We performed a detailed numerical simulation to analyze and optimize the high-frequency performance of FEDs. We use the cut-off frequency (the frequency at which the current gain is 1) to describe the high-frequency of a device.

The cut-off frequency of the intrinsic transistor without parasitic capacitance is

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_G} \quad (2)$$

where $g_m$ and $C_G$ are transconductance and gate capacitance, respectively. The transconductance, $g_m$, is calculated from simulation results by

$$g_m = \frac{\partial I_{DS}}{\partial V_G} \quad (3)$$

Fig.5 shows $g_m$ as a function of the $L_{sp}$ for S-FED and M-FED. Fig.5 illustrates that by increasing the $L_{sp}$, the transconductance decreases. As can be seen in this figure, by increasing $L_{sp}$, the frequency response increases.

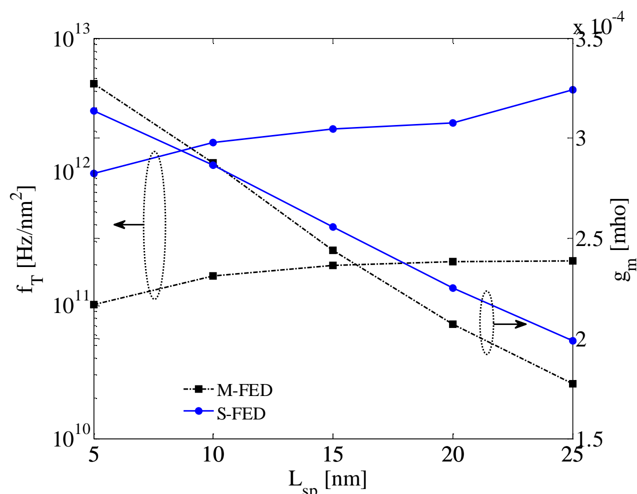


**Fig. 5**. The frequency response and transconductance of FEDs as a function of $L_{sp}$.

## 3. Conclusion

The role of the spacer length between gates on the performance of M-FED and S-FED has been investigated. Our results indicate that by appropriate selection of the spacer length, the $I_{on}/I_{off}$ ratio can be increased to $10^4$ for S-FEDs. The high-frequency performance of FEDs is investigated and the cut-off frequency of the intrinsic transistor without parasitic capacitance is calculated. Important figures of merit of FEDs for digital applications have been studied. Results demonstrate that FEDs can be considered as interesting candidates for future digital applications. The results reported herein provide a facile and with desired properties.

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