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RESEARCH PAPER

Performance Improvement of Double Gate Nano-TFET Via Combination of Dual Material Gate-Drain Overlap and Source Pocket

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ABSTRACT

Although tunneling field effect transistors (TFETs) exhibit low threshold swing and enable good scalability, but TFETs suffer from two main problems: low ON-state current (I_{ON}) and intrinsic ambipolar conduction. In this work, we propose a structure of double-gate TFET with 50nm channel length, which has lower ambipolar conduction and higher ON-state current compared to conventional double-gate TFET. In the proposed TEFT, in order to achieve the minimum ambipolar conduction, dual material gate (DMG) has been integrated with the gate-drain overlap (GDO), and in order to simultaneously improve the ambipolar conduction and the ON-state current, the source pocket (SP) has been added to the structure. We show in proposed device, by increasing the length and thickness of the source pocket, the ON-state current increases. In addition, increasing doping of the source pocket shows enhanced ION order up to 4E-3. We compare 4 TFET structures, namely DG-TFET, DMG-DGTFET, GDO-DMG-DGTFET, and the proposed structure (SP-GDO-DMG-DGTFET). We show that the proposed structure has a higher I_{ON}/I_{OFF} ratio (1E14) and less ambipolar conduction than other structures under study and is more suitable for digital applications. Also, by calculating transconductance (g_m), gate-drain capacitance (C_{gd}), gate-source capacitance (C_{gs}), we show that the proposed structure has the highest cut off frequency (0.6THz) compared to other structures under study and is more suitable for high frequency applications.

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INTRODUCTION

One of the major problems to continue the scaling process of the CMOS devices is the power consumption. Scaling of transistors and increasing the density of transistors on the chip increases the power density on the chip. Therefore, according to the scaling of the transistors, the supply voltage should be reduced. Although scaling the supply voltage reduces dynamic power consumption, but to achieve the same ON-current, the threshold voltage must be scaled as the supply voltage decreases. Decreasing the threshold voltage leads to an exponential increase of OFF-state current and the static power. The exponential increase of OFF-state current is due to threshold swing limit of 60 mV/decade, which is caused by the thermal carrier

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injection mechanism [1]. The carrier transmission mechanism in TFETs (tunneling field effect transistors) is based on band-to-band tunneling (BTBT), so they have low subthreshold swing compared to MOSFET and are the most promising devices for low-power applications [2-3-4-5-6]. Although TFETs can overcome the theoretical limit of subthreshold swing of conventional MOSFETs and can be used in ultra-low voltage circuits that are very energy efficient, but they face two major problems: low ON-state current and ambipolar conduction.

The tunneling probability of the carriers is reduced due to the large tunneling resistance in the TFET. As a result, the ON-state current of TFET is significantly lower than of the MOSFET [7-8]. To enhance the ON-state current of TFET, some researches have been done, for example: using III-V compound semiconductor [9-10-11], using high-k gate oxide (HfO2) [12-13], increasing the tunnel area [14], using dual source region [15], increasing the source doping concentration [16]. Also, an abrupt source doping profile increases I_{ON} [17]. In addition, the ON-state current of the double-gate TFET is greatly improved compared to the conventional single-gate TFET [18-19]. This is due to the high dependence of the barrier width on the gate voltage, and consequently the width of the barrier can be better controlled by using double gates in the TFET.

Another disadvantage in TFETs is the presence of ambipolar conduction. Ambipolarity is an intrinsic phenomenon of TFET technology where the conduction occurs for both positive and negative gate voltages. The ambipolar current (I_{amb}) flows due to BTBT at the channel-drain junction for negative gate voltage for n-type TFET, and positive for p-type, which makes TFET technology unsuitable for complementary logic digital systems [20]. Fig. 2 shows the schematic representation of inverter using complementary TFETs. When a low voltage is applied to the input, the N-TFET is expected to be off and the output voltage will be equal to VDD, but due to the ambipolar conduction of the N-TFET, the output voltage will be less than VDD, for high V_{IN}, the ambipolar conduction of P-TFET switches on and so output voltage cannot reach 0V [21-22]. And this means that ambipolar conduction leads to incorrect operation of logic gates. In order to reduce the ambipolar conduction, some ways have been proposed, such as: spacer and contact engineering [23-24], non-uniform drain doping [25], using dual material gate dielectric [26], overlapping of the gate on the drain region [27-28]. Also, the tapered channel structure with a higher thickness at the source side, has reduced the ambipolar conduction [29].

In the present work, we show in several structures how the combination of dual material gate with drain gate overlap and source pocket insertion can reduce the ambipolar current and increase the ON-state current of a conventional DG-TFET. Also, by calculating I_{ON}/I_{OFF} ratio, transconductance (g_m), gate-drain capacitance (C_{gd}), gate-source capacitance (C_{gs}), and cut-off frequency, we show that the proposed structure increases the device figures of merit for digital and high frequency applications. This paper is organized as follows: In first section, the device structures and simulation models are presented. In the next section, the electrical characteristics of the studied device structures are discussed. And then, the effect of different parameters on the proposed structure operation is investigated. Finally, a summary of the results of this article is presented.

DEVICES STRUCTURES AND SIMULATION PARAMETERS

The four different structures of double gate Tunnel-FET (DG-TFET) under study, are shown in Fig. 1. The first structure (I), is a conventional DG-TFET. In the second structure (II), both upper and lower gate metal are engineered with dual material (DMG-DGTFET). That gate work function near the drain side (auxiliary gate) is lower than gate work function near the source side. In third structure (III) the dual material gate combined with gate-drain overlap (GDO-DMG-DGTFET). So that the length of the auxiliary gate has been overlapped on drain by 42nm. The fourth structure (IV), which is the proposed structure, is similar to the third structure, with the difference that the n+ Source Pocket has been added in the fourth structure (SP-GDO-DMG-DGTFET).

The simulation parameters of the structures are presented in Table 1. In this work the simulations are obtained using TCAD SILVACO. There are different tunneling models available in TCAD tools. The choice of tunneling model plays the most important role in the accuracy of the results obtained from the TFET simulation. We have used the non-local tunneling model which can

accurately represent the tunneling physics. In non-local tunneling models, the possible tunneling paths are identified by the simulator and the tunneling probabilities, For the given tunneling path and the given profile of the energy bands are computed by employing techniques like Wentzel-Kramer-Brillouin (WKB) approximation or more rigorous quantum treatment. Also, we have used the band gap narrowing (BGN) model to calculate heavily doped regions in the devices. In order to consider the rate of generation/recombination we have used Shockley-Read-Hall (SRH) and Auger models. We have also used drift diffusion carrier transport model and Fermi Dirac distribution function model. The model has been calibrated using the data of the silicon DG-TFET of the Ref

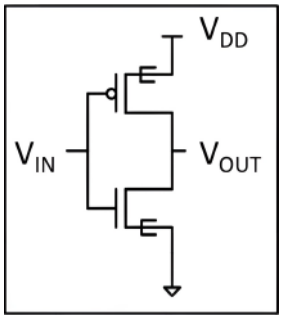

Fig. 1. the inverter using complementary TFETs, that ambipolar conduction in TFET leads to incorrect operation of inverter.

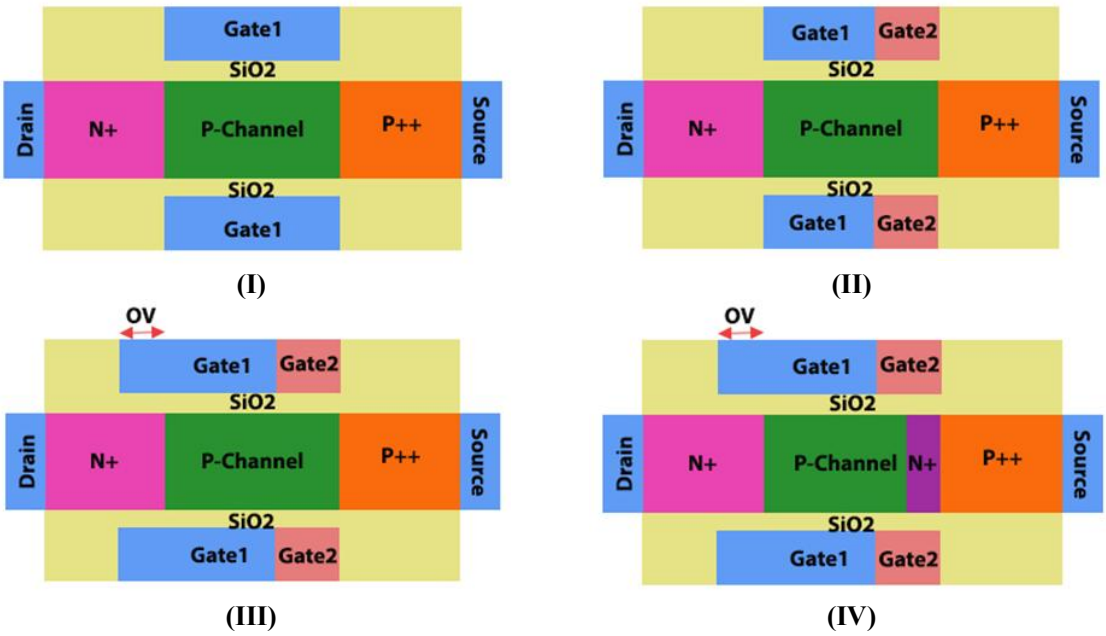

Fig. 2. A schematic of the studied DG-TFET. (I) the conventional DG-TFET, (II) the DGTFET with dual material gate (DMG-DGTFET), (III) the DGTFET with combination of dual material gate and gate-drain overlap (GDO-DMG-DGTFET), (IV) the DGTFET with combination of dual material gate and gate-drain overlap and source pocket (SP- GDO-DMG-DGTFET).

[30] and based on the effective mass.

RESULTS AND DISCUSSION

Fig. 3 shows the transfer characteristic of five structures at V_{DS}= 1V. Conventional TFET has the highest ambipolar conduction compared to other studied structures. In the second structure, using two gate materials and insertion a material with a lower work function on the drain side has reduced the ambipolar conduction to 1E-1o. In

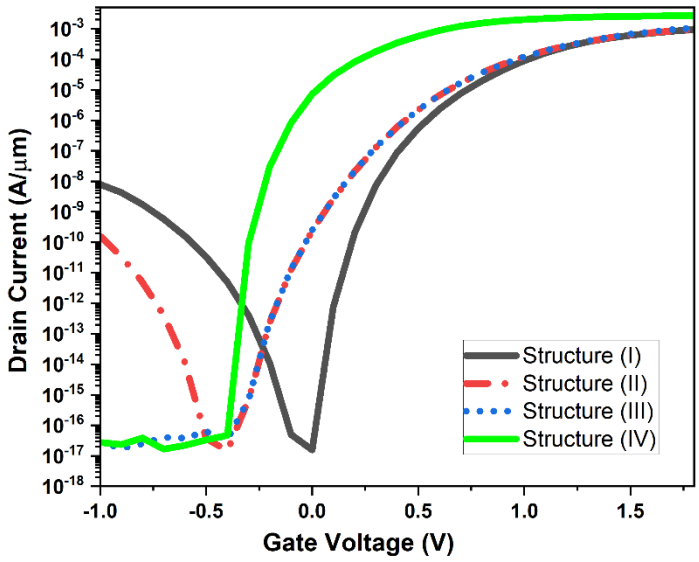

Fig. 3. The transfer characteristic of five structures at VDS=1.0 V.

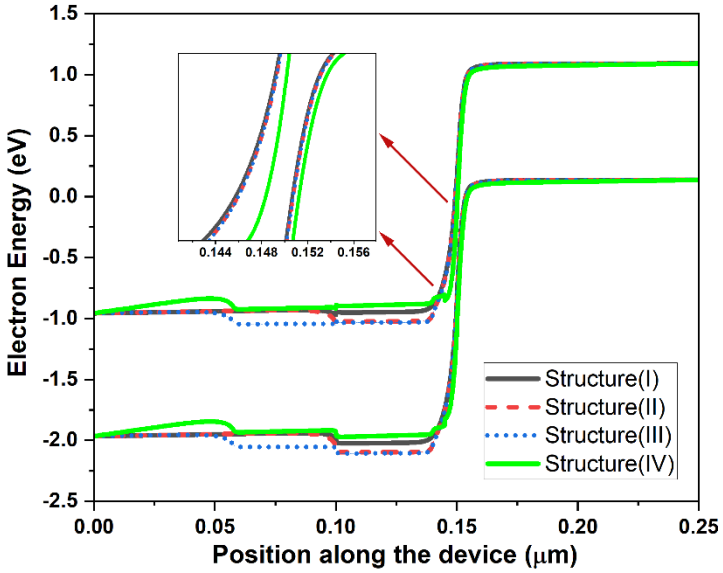

Fig. 4. The energy band diagram of four structures at V_GS=1V and V_DS=1V.

the third structure, the simultaneous use of two gate materials with the gate-drain overlap, has led to a significant decrease in ambipolar conduction to 5E-17. In the fourth structure, adding the source pocket has increased the ON-state current. Meanwhile, the ambipolar conduction in this structure is maintained at 5E-17. Consequently, for the case of SP-GDO-DMDG-TFET, both I_{ON} (enhanced) and the I_{amb} (reduced) have been improved.

In order to analyze the behavior of the transfer characteristics, the energy band diagram of the structures has been extracted in Fig. 4 and Fig. 5. According to the Wentzel-Kramer-Brillouin (WKB) approximation, the tunneling probability T(E) is calculated using [31]:

$$T(E) = \exp\left(-2\int_{x_{start}}^{x_{end}} k(x)\,dx\right) \quad (1)$$

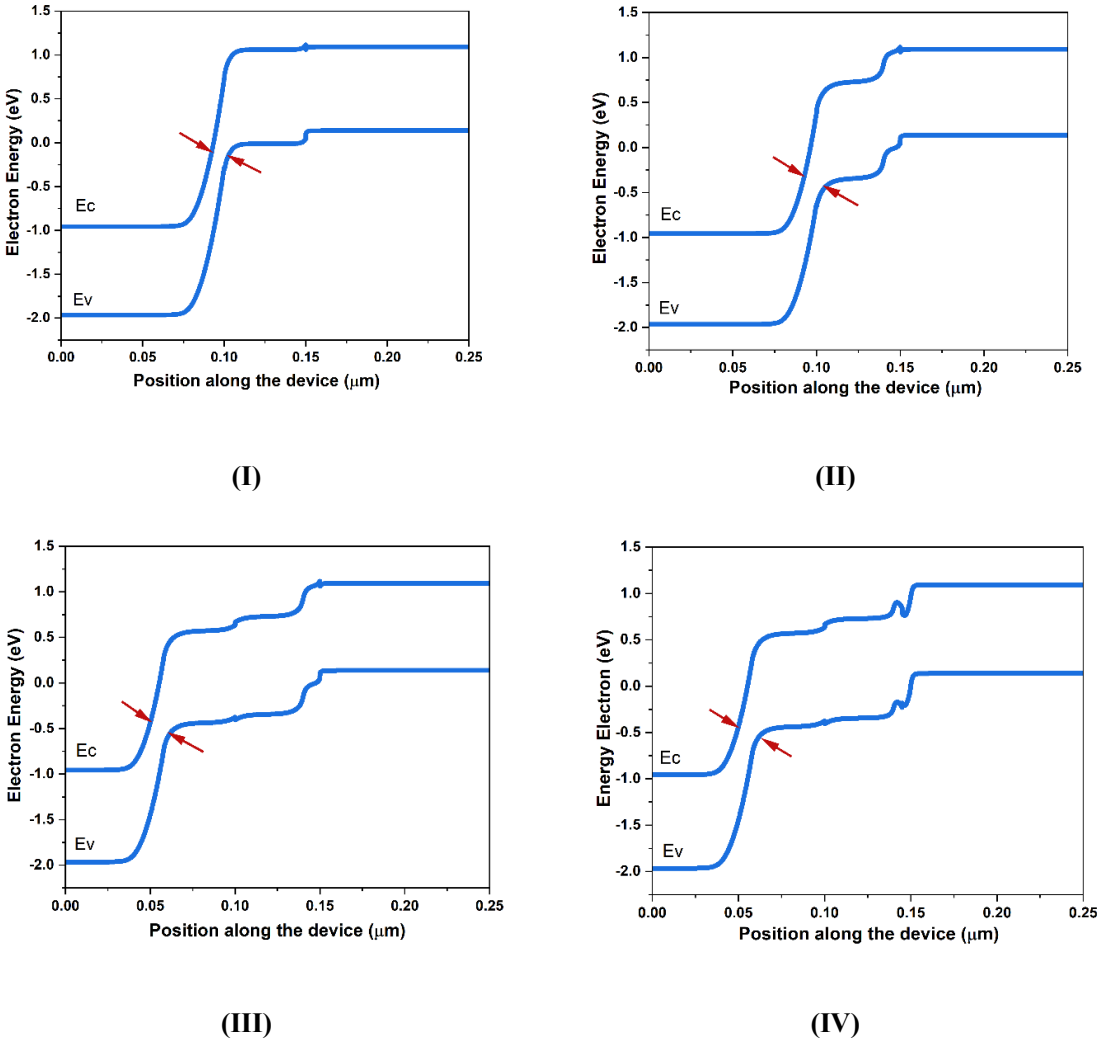

Fig. 5. The energy band diagram of four structures at V_GS=-1V and V_DS=1V. (I) the conventional DG-TFET, (II) the DGTFET with dual material gate, (III) the DGTFET with combination of dual material gate and gate-drain overlap, (IV) the DGTFET with combination of dual material gate and gate-drain overlap and source pocket.

where k is the wave vector and x_{start} and x_{end} points are the start and end points of the tunneling path. This equation shows that for a narrower tunneling path, the tunneling probability increases.

Fig. 4 depicts the energy band diagram of four structures at V_{GS} =1V and V_{DS} =1V. In the fourth structure, the tunneling width at the source-channel junction, is less compared to the other three structures, so according to the above theorem, the tunneling probability is higher than other structures and as a result, it has a highest ON-state current. In other structures, the tunneling width appears to be the same and thus have the same I_{ON}.

Fig. 5 shows the energy band diagram of four structures at V_{GS} = -1V and V_{DS} =1V. In the n-type TFET device, if the gate voltage is sufficiently negative, ambipolar conduction is created, so that in negative gate voltages the edge of the channel valence band is placed above the edge of the drain conduction band, and the narrowing of the tunneling barrier at the channel-drain junction enables the tunneling from channel to drain. In

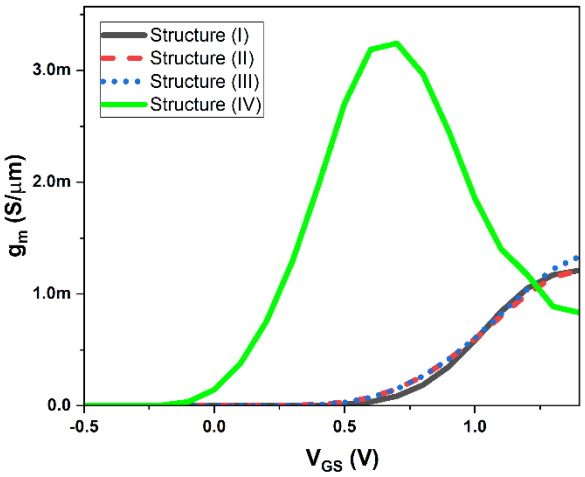

Fig. 6. The transconductance of four structures.

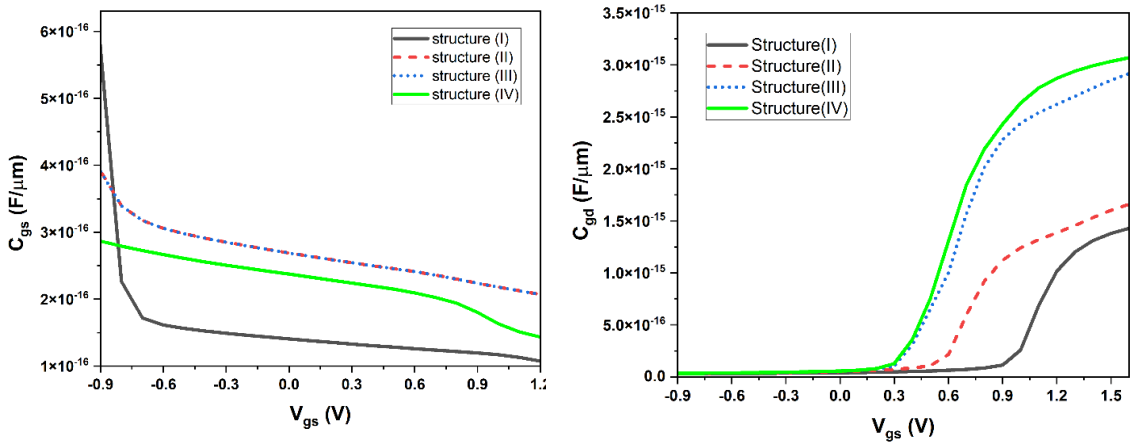

Fig. 7. The Parasitic capacitances. (a) gate-source capacitance, (b) gate-drain capacitance.

Fig. 5, the tunneling barrier width at channel-drain junction, is specified. It can be seen that in the first structure, the tunneling barrier width is less than other structures. And therefore, structure (I) has the highest tunneling probability and highest ambipolar conduction. In the second structure, the tunneling barrier width has decreased compared to structure (I), so the ambipolar conduction is reduced in the second structure. The third and fourth structures have the lowest tunneling barrier width and therefore have the lowest ambipolar conduction.

In TFETs, the gate voltage controls the current, and therefore, the I_{DS}/V_{GS} ratio at constant drain bias, defined as transconductance, becomes an important parameter for TFETs [32]. To obtain high gain or high driving capability, g_m should be high. The transconductance of All the device structures investigated are shown in Fig. 6. A significant improvement in gm is achieved by adding source pocket in the SP-GDO-DMDG-TFET as shown in Fig. 6.

In order to analyze the high frequency performance, the cutoff frequency of all structures

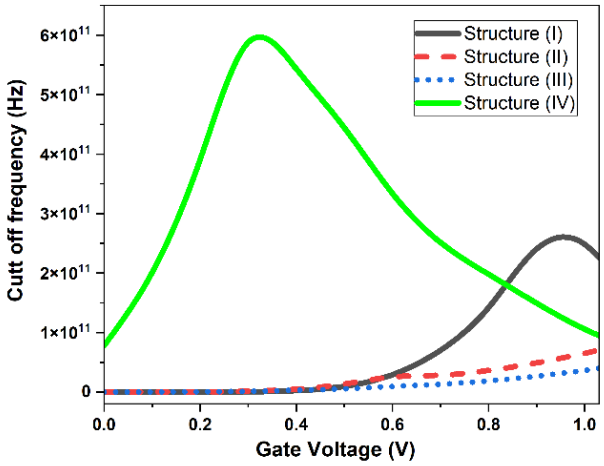

Fig. 8. The cutoff frequency of four structures.

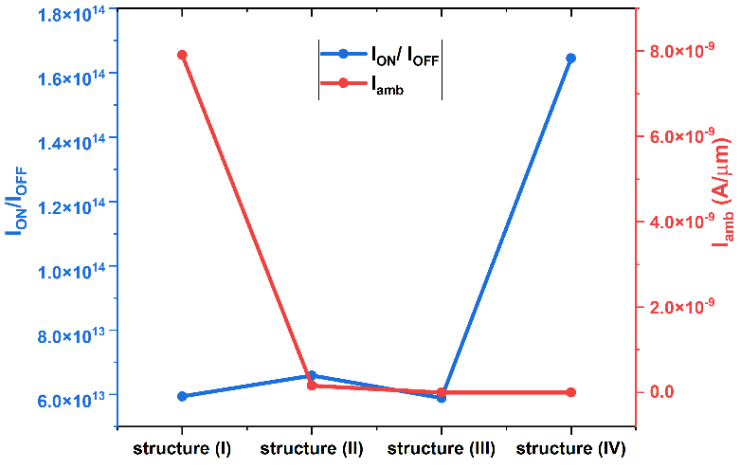

Fig. 9. the I_{ON}/I_{OFF} ratio and ambipolar conduction of all the devices under investigation.

is studied. Cutoff frequency is defined as the frequency at which the short circuit current gain drops to 0 dB, and it is expressed as [33]:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (2)$$

where g_m is the transconductance, C_{gs} and C_{gd} are gate-source and gate-drain capacitances. As can be seen from the equation, the cutoff frequency depends directly on g_m and inversely on the parasitic capacitances. Parasitic capacitances reduce the cutoff frequency and limit the switching speed. In this work, dual metal gate and gate-drain overlap techniques were used to reduce the ambipolar conduction of TFET, and therefore it is necessary to investigate the effect of dual metal gate and gate-drain overlap and source pocket engineering on parasitic capacitances. The parasitic capacitances of structures including gate-source capacitance and gate-drain capacitance are shown in Fig. 7.

It is evident from Fig. 7 that dual material gate

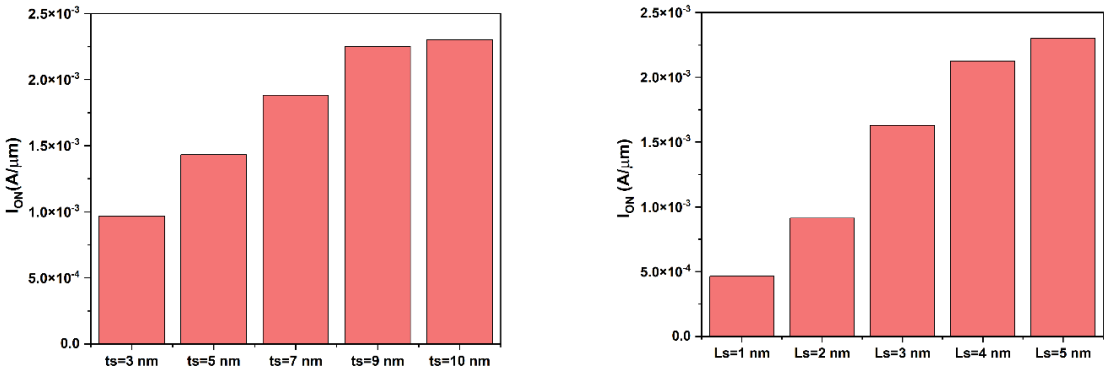

Fig. 10. the effect of source pocket parameters. (a) the thickness of source pocket, (b) the length of source pocket.

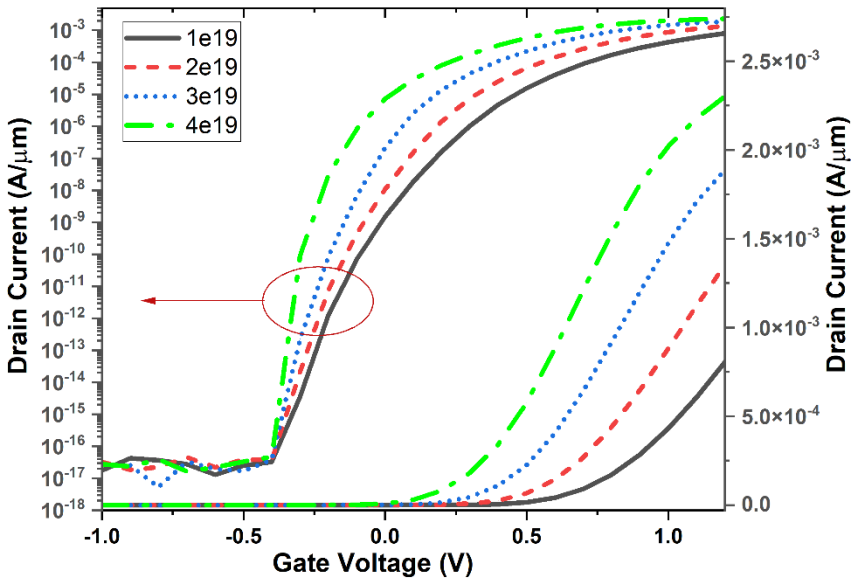

Fig. 11. the effect of source pocket concentration on structure (IV).

and gate-drain overlap techniques has made the parasitic capacitances worse than the conventional TFET.

In order to overcome the degradation in the cutoff frequency caused by dual metal gate and gate-drain overlap, we have added the source pocket to the structure. Adding the source pocket in the proposed structure has led to increase g_m and has overcome the effect of increasing parasitic capacitances. In Fig. 8, the cutoff frequency of the structures is calculated, as it is evident the overcoming gm has resulted a Preeminent cutoff frequency for the SP-GDO-DMDG-TFET. So that by adding the SP technique, the f_T peak value has increased from 250 GHz in the conventional DGTFET to 600 GHz.

Fig. 9 depicts the I_{ON}/I_{OFF} ratio and ambipolar conduction of all the devices under investigation. The excellent I_{ON}/I_{OFF} ratio (1E14) and suppressed ambipolar (5E-17) conduction make the SP-GDO-DMG DGTFET an supreme device for digital applications.

The effect of thickness, length and doping value of source pocket on the performance of structure (IV) is investigated. Fig. 4 shows the effect of changing the length and thickness of the source pocket on the ON-state current. As we can see, the I_{ON} increases with the increase of length and thickness of source pocket.

Fig. 11 shows the effect of the source pocket doping concentration on the structure (IV). It can be seen that increasing of the source pocket doping concentration, clearly increases the ON-state current.

CONCLUSION

In this paper, a structure of DG-TFET was proposed which improves the electrical characteristics of conventional DGTET. We have shown that the integration of dual material gate with gate-drain overlap can significantly reduce the ambipolar conduction. And adding the source pocket to the proposed structure, increases ON-state current. So that the proposed structure has a high I_{ON}/I_{OFF} ratio (1E14) and the lowest ambipolar conduction (5E-17). We showed that the gate-drain overlap worsens the effect of parasitic capacitances, but in the proposed structure, adding the source pocket leads to high gm in the proposed structure, which dominates the effect of parasitic capacitances. So that the proposed structure has a high cut off frequency (600GHz) and is very suitable for high frequency applications.

CONFLICT OF INTEREST

The authors declare that there is no conflict of interests regarding the publication of this manuscript.

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