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RESEARCH PAPER

Impact of nano-Scale Statistical Variability on SRAM Stability: A Comparative Study between 6T and 8T Cells

Hamed Tasdighi [1], *Daryoosh Dideban* [1,2] *

[1] *Department of Electrical and Computer Engineering, University of Kashan, Iran*

[2] *Institute of nano-Science and nano-Technology, University of Kashan, Iran*

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ABSTRACT

Nano scale statistical variability which arises from discreteness of charge and granularity of matter has become one of major concerns in digital design particularly in sub-50nm technology nodes. Device intrinsic parameters such as the threshold voltage and drive current will be influenced by random dopants, line edge roughness and gate grain granularity which in turn results in variation of SRAM cell performance. Therefore, providing an accurate statistical model is one of the key issues among SRAM design community. Since both 6T and 8T SRAMs are widely used in the industry as standard cells, this article analyzes sensitivity of static noise margin (SNM) in response to statistical variations in 6- and 8-transistor cells. The results show that though 8T cells need more transistors and thus consume more area on the wafer compared with 6T cells, they are more stable and thus are better candidates for variability aware design in future technology nodes.

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INTRODUCTION

Statistical variation is among important issues which are caused by transistor scaling in advanced technologies. Therefore, analysis and modeling of these variations is a vital issue in achieving proper circuit performance [1,2,3]. The impact of these variations on SRAM cell transistor causes stability concerns, which should be taken into account early in design stages. However, a rotational mode never merely appears under certain conditions and the cells are referred to as “weak cells” with insufficient noise margin due to such instabilities [4,5].

This article presents a new statistical model SNM of a cell in response to statistical variations. This method (Monte Carlo simulation method based on ‘atomistic’ results) is highly accurate because BSIM4 HSPICE modelcards which are used in the Monte Carlo simulations are directly extracted from numerical simulation of nano-MOSFET devices, taking into account quantum confinement effects inside drift-diffusion current formulations. In this method, we have used 1000 samples of n and p-channel MOSFET transistors with the gate length of 35nm and a unique structure of statistical parameter fluctuations (PDF,LER, and PGG) are used in the process of Monte Carlo HSPICE simulation. In fact, 1000 random netlist files were generated for HSPICE simulator and each file is an SRAM cell with unique structure of intrinsic parameters. SNM was then extracted for any output file, which enables us to analyze mean and standard deviation of SNM along with its statistical properties.

* *Corresponding Author Email: dideban@kashanu.ac.ir*

Fig. (1-a) shows the Monte Carlo process flow as the main structure of statistical simulation simulation. Fig (1-b) illustrates a 6T-SRAM cell which is made of two reciprocally connected inverters and two access transistors. M1 and M2 are the driver transistors with the maximum role in maintaining data in a cell. M5 and M6 are the pull-up transistors which are used as a load for M1 and M2. M3 and M4 are the access transistors, which are responsible for reading data from a cell and writing data in a cell. As Figure (1-c) shows, 8T-SRAM cell is similar to the 6T cell with

addition of two transistors, M7 and M8, where they provide access to data stored in this cell different than a 6T cell [6]. Moreover, authors in [7-12] proposed a variety of techniques to study the impact of statistical variability on digital circuits and systems.

The paper is organized in 4 sections: section 2 investigates the impact of threshold voltage variation on both 6T and 8T cells. Section 3 presents statistical models of both cells in response to supply voltage variations. Section 4 provides the study of impact of aspect ratio of driver transistors on SNM of both cells. Impact of statistical fluctuations in the worldline voltage on SNM is discussed in section 5. Finally, a conclusion is presented in section 6.

Threshold voltage variations

Since the nature of intrinsic fluctuations is random, they can only be expressed using their statistical distribution. This is a notable point in designing nano-scale ICs and one of the major issues in circuit performance and its reliability. Random variations sources including RFD, LER, and PGG are the major causes of threshold voltage variations particularly for MOSFETs with sub-40nm channel lengths [14].

Variations in V_{TH} of driver transistors have the greatest impact on the stability of cells, which is caused by greater proportion of W/L as compared with other cell transistors.V_{TH} of driver transistors reduces with increased V_{bs}. Non-destructive maintenance condition of an SRAM cell increases leakage current of this transistor and enhances the stability. Increased V_{bs} in access transistors reduces V_{TH} of the transistor and makes easy access to a cell. For this reason, access transistors and load are shunted strongly in each cell accessed for reading and writing data. They expose the low mode of a cell to a destructive effect [15].

Fig. 2 (a) shows SNM standard deviation for V_{TH} (or equivalently V_{bs}) of driver transistors in both cells. As type of access to the cell is different in 8T cell, its stability exceeds 6T cell and the variations in VTH of access transistors has less effects on cell stability. As access to data only depends on two access transistors in the 6T cell, variations in V_{TH} of access transistors cause further deviation as compared with 8T cell in cell stability. Fig.2 (b) shows the standard deviation in which deviation in V_{bs} of driver transistors of 8T cell (65%) and access transistors in this cell (15%) respectively cause the maximum and minimum deviation in the standard deviation of SNM. Fig.2 (c) shows the SNM skewness. For the above reasons, deviations of the driver transistors exceed the access ones.

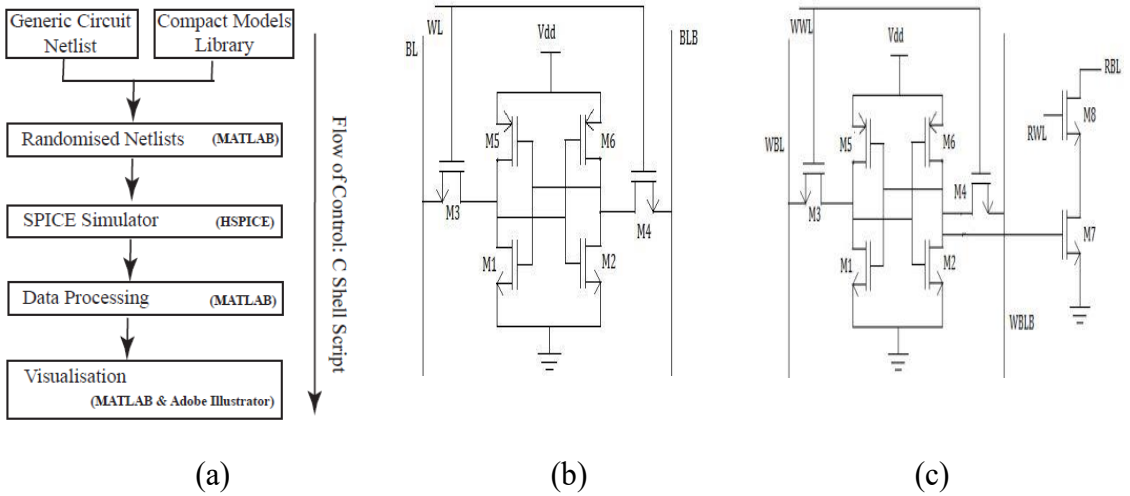

Fig. 1. (a)- Monte-Carlo simulation process [13], (b)-SRAM 6T cell, (c)- SRAM 8T cell

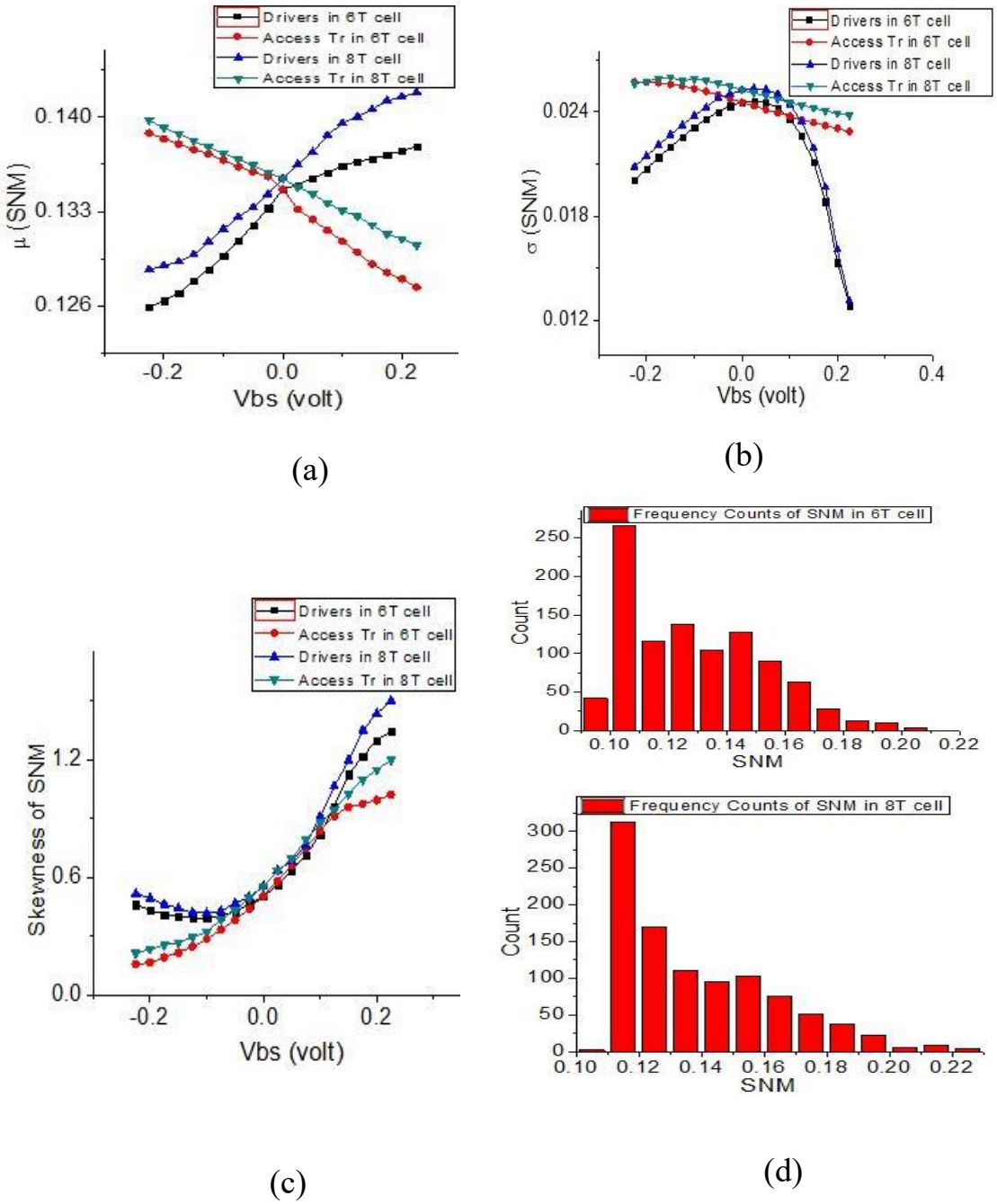

Fig. 2. Impact of threshold voltage (or equivalently V_{bs}) variations on: (a)-SNM mean, (b)-SNM standard deviation, (c)-SNM Skewness, (d)- SNM distribution.

Fig. 2 (d) compares SNM distribution with 40% deviation in V_{TH} of access transistors in 8T and 6T cells and shows superiority of 8T cell to 6T cell in data stability.

Supply voltage variation

These variations are caused by other network emissions and the surrounding environment as noise superimposed on the supply. Supply voltage

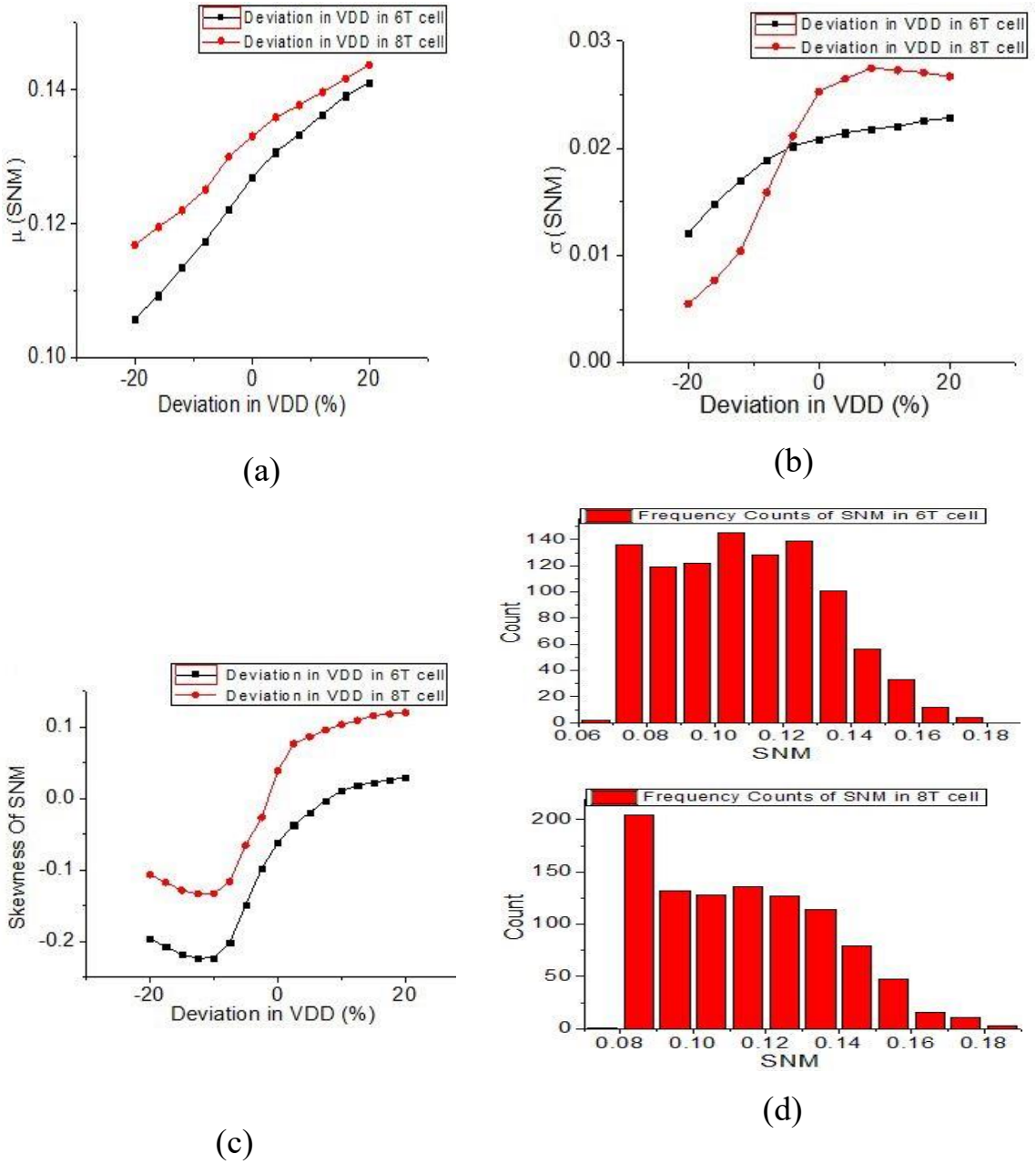

Fig. 3. Impact of supply voltage variations on: (a)- SNM man, (b)- SNM standard deviation, (c)- SNM Skewness, (d)- SNM distribution.

variations are introduced as an error through the supply voltage network of an SRAM cell. SNM shows a strong dependency on cell supply variations, as wordline voltage and global bit lines in V_{DD} are complete. This makes an access transistor shunt pull-up transistors strongly and affect the cell's low mode in a destructive manner [16]. As Fig.3(a) shows, supply voltage variations have a significant effect on SNM mean value, and SNM mean values in 8T cell exceed 6T cell. In the standard deviation as shown in Fig.3(b), supply deviations in the 8T cell have a further impact on the standard deviation of SNM as compared with the 6T cell.

Gradient of variations in the third momentum of SNM is illustrated in Fig.3(c). It shows similar trend in both cells and this similarity of gradient is caused by the fact that both cells can access to

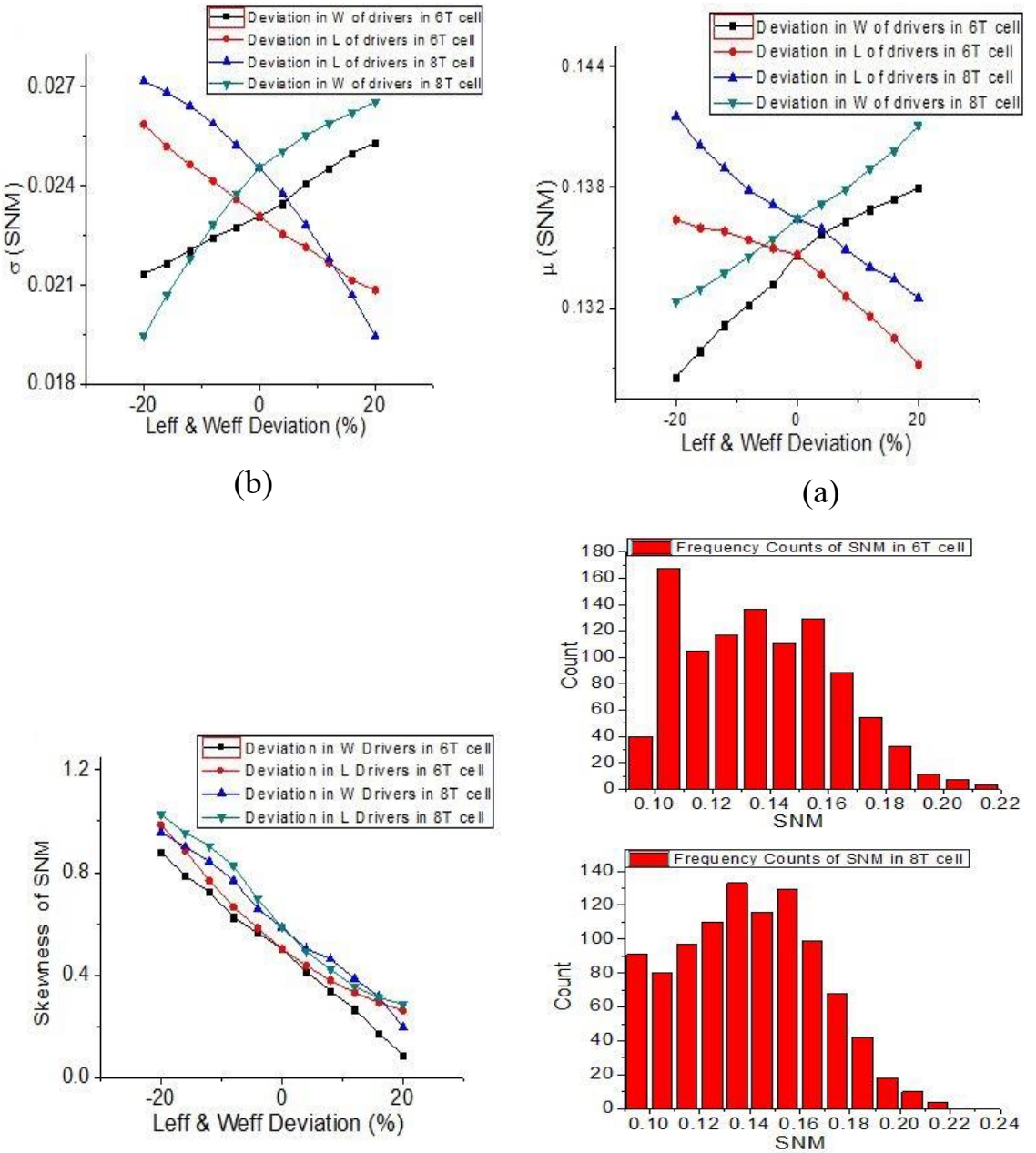

Fig. 4. The impact of W/L of driver variations on: (a)- SNM mean, (b)-SNM standard deviation, (c)- SNM Skewness, (d)- SNM distribution.

data in similar fashion. In this condition, both cells are accessed for reading, wordline voltage and global bit lines in V_{DD} are complete, and variation only occurs in supply of the two inverters, which are connected reciprocally and thus preserve data. Fig. 3(d) shows SNM distribution for 15% of variation in supply voltage for both cells, while 8T cell represents slightly higher SNM.

Variations in driver transistor aspect ratio

To assure non-destructive reading, sufficient noise margin, and preservation of a reasonable SNM and efficiency in SRAM cells utilizing CMOS technology, cell ratios should be increased from the usual rate of (W/L)Drivers/((W/L)Access Tr)=2 to higher ratios in order to preserve scaling balance in advanced multi-ten-nanometer technologies [10]. Due to increased W/L ratio of

driver transistors compared with other transistors in the cell, we only study the effect of variations in W/L ratio of the driver transistors on SNM of two cells.

Fig. 4(a) shows the dependency of SNM mean of 6T and 8T cells on W_{eff} and L_{eff} variations of driver transistors. SNM reduction is significant when the variation in the length and width of the driver transistor reaches to 20% of the typical values. Analysis of Fig.4(a) reveals the fact that the 8T cell is more stable than the 6T cell. Transistor width increase in both cells results in cell ratio increment and thus leads to SNM improvement. With the L of driver transistors increasing in the

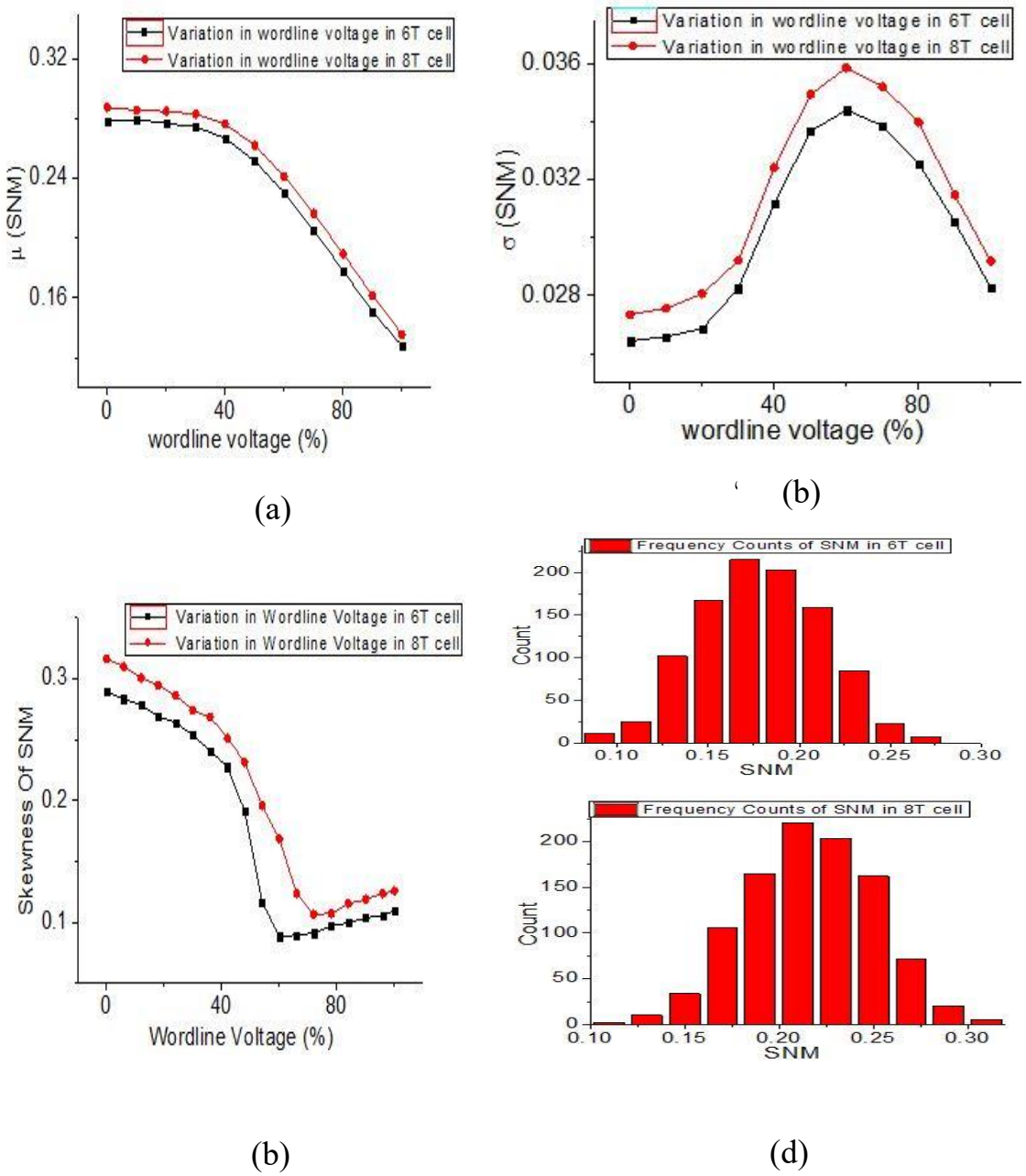

Fig. 5. The impact of supply voltage variation on: (a)-SNM mean, (b)-SNM standard deviation, (c)- SNM Skewness, (d)-SNM distribution.

cells, cell ratio decreases and it reduces SNM. The standard deviation in Fig.4(b) shows that the variations in W/L ratio of 8T cell cause further deviation in the second momentum of SNM. Fig.4(c) shows skewness and SNM for variations in W/L ratio of both cells in which gradient and variation ratio of both cells are almost equal. Fig. 4(d) shows SNM distribution for 20% reduction in L of driver transistors in both cells, which indicates higher noise margin of 8T cell.

Wordline voltage variation (Vwl)

If $Vwl<V_{TH}$ in an access transistor, it has no effect on SNM and it is an isolated cell from read and write drivers. As soon as $Vwl\geq V_{TH}$ in the access transistor, the cell is accessed for reading or writing, and access transistors start shunting load transistors and lifting the node that saves low mode and reducing SNM considerably [17]. As Fig.5(a) indicates, 8T cell manifests a higher noise margin in response to V_{WI} variations and with the increased voltage in both cells, SNM wordline will significantly be decreased. An interesting phenomenon is observed in Fig.5(b) where the SNM standard deviation occurs in 60% of the typical value of worldline voltage (Vwl) in which the voltage reaches the access transistor's threshold voltage and the cell is accessed for either reading or writing. The SNM skewness in response to worldline variations follows the same trend as shown in Fig.5(c) with slightly more values for 8T cell. Fig. 5(d) shows SNM distribution while the voltage (Vwl) is in 60% of its typical value in each cell, which indicates superiority of 8T cell over 6T cell as far as stability is concerned.

CONCLUSION

With respect to technological advancements and thus increase of random variations, manufacturing ICs without considering statistical variations in the design stage is a waste. Thus, variability aware design is essential to help designers with useful statistical circuit models. This paper performed an extensive analysis of SNM sensitivity in both 6T and 8T cells to identify the statistical distribution of weak cells with insufficient noise margin for each circuit configuration. The stability analysis and comparison was carried out between 6T and 8T cells against different statistical variations. In all cases, 8T cell's SNM was higher than that of 6T cell as far as stability was concerned. However, as far as area and size were concerned, 6T cell is superior as it utilizes fewer transistors. Therefore, exact selection of one particular cell depends on the tradeoff between circuit size and SNM, which is indeed based on a target application needs.

CONFLICT OF INTEREST

The authors declare that there are no conflicts of interest regarding the publication of this manuscript.

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